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BUS INTERFACE UNIT LSI CHIP DEVELOPMENT

Harris Corporation
Government Information
Systems Division
Melbourne FL 32901

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Final Technical Report

August 1981

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20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

This report describes a large scale integrated (LSI) circuit implementation of the MIL-STD-1553B serial data bus protocol. Two chips were designed to achieve all of the data bus interface functions. Chip type #1 is concerned with sync generation/detection, encoding/decoding, terminal address/subaddress recognition, direct memory access (DMA) functions, first level error detection, and some mode code responses. This chip was produced in CMOS technology and is available from Harris Corporation. Chip type #2 was concerned with the more complex bus controller functions including command word generation, data

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buffer address generation, time tagging of data, control codes, programmed interrupts, working registers, mode code responses, and second level error detect functions. Chip type #2 was breadboard in TTL circuits but was not produced in LSI silicon.

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TABLE OF FIGURES

1.0 BUS INTERFACE UNIT (BIU)

1.1 General Description

The BIU is an LSI approach to implementation of the interface between a host electronics and a manchester data bus. With such an interface, a group of up to 31 hosts can transfer information between each other on the serial data bus. Figure 1.1-1 illustrates BIU usage.

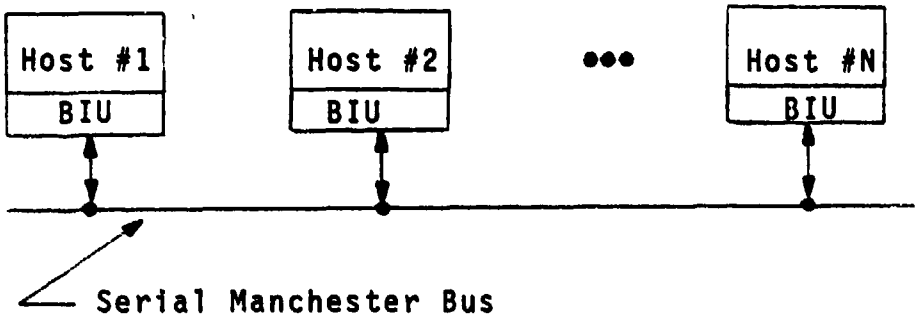

FIGURE 1.1-1
SYSTEM USE OF THE BIU

At the manchester bus interface the BIU accepts serial bi-phase data or generates serial bi-phase data. At the host electronics interface the BIU accepts instructions from the host, and by way of these instructions, transfers parallel data to and from the host. Within a host box, the BIU resides between a transmitter/receiver unit and the internal, parallel data and address buses as shown in Figure 1.1-2.

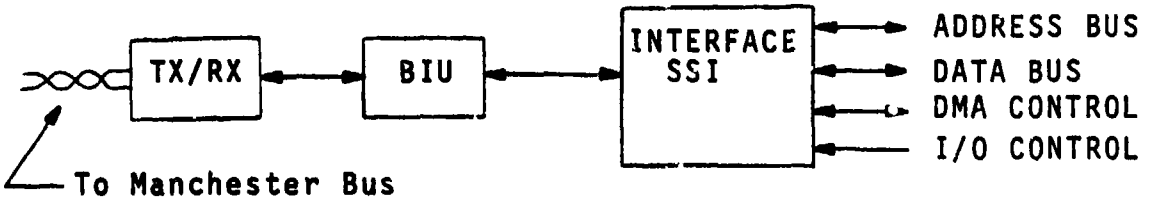

FIGURE 1.1-2
BIU WITHIN THE HOST BOX

MIL-STD-1553B forms the protocol basis for the BIU. Within 1553B, the hosts relate to each other as "remotes" or "controllers". At any one instant, one host is recognized as the controller, all the remaining hosts are considered remotes. Provision is made in 1553B and the BIU to allow for dynamic reassignment of these roles.

As a remote, the BIU is first programmed by its host through the use of I/O control transfers. Then, the BIU is capable of carrying out data transfers to and from the host memory via DMA. In this situation the BIU is stimulated by command words from the data bus.

As a controller, the BIU is first programmed by its host as above. After programming, the BIU is capable of executing the stored program code in host memory. This allows the BIU to develop the appropriate bus commands and handle data associated with these commands. This also allows the BIU to handle automatic retries and to pass interrupts to the host when retries fail or other conditions warrant.

In summary, the BIU off-loads the bus interface function from the host in either remote or controller situations and acts as an integrated DMA channel between the serial bus and host memory.

Physically, the BIU is contained in two LSI chips. In the most elemental applications, Chip #1 can be used without Chip #2. This is especially true if the selected host will never assume the role of controller. A basic block diagram of BIU #1 is given in Figure 1.1-3. Referring to the figure, some of the control lines allow for initialization and for the transfer of words (command words, status words, and error words) through the chip's I/O interface. Other control lines (the DMA controls) allow for the transfer of data words through the I/O. A functional pinout is given in Figure 1.1-4.

Figure 1.1-5 illustrates BIU #1 embedded in a simple host. Referring to the figure, the various logic elements are assumed CMOS compatible and connect directly to the BIU. The application is set up with output registers ready to accept data from the BIU when it outputs data on its I/O bus. Data is supplied to the BIU's I/O bus when requested through input tri-state buffers. The flow of data is controlled by word count decodes and the read and write lines. The binary-to-unitary decoder (e.g., CD4028B) converts the word count into discrete lines which select both an input tri-state buffer and an output register. Input or output is then determined by an active read or active write. To satisfy the DMA handshake requirements in

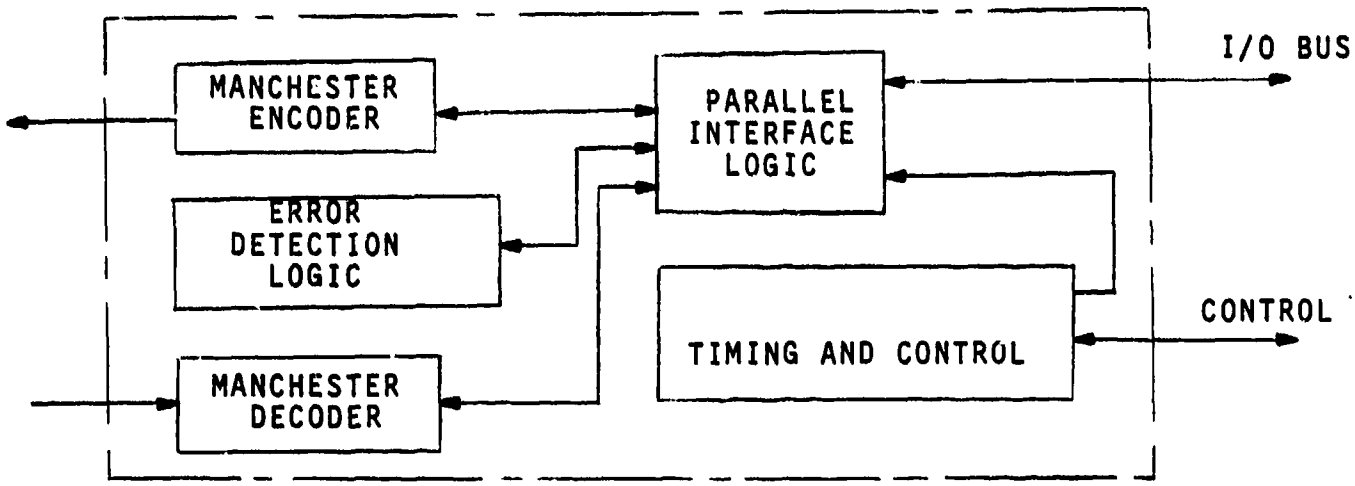

FIGURE 1.1-3
BASIC BLOCK DIAGRAM OF BIU #1

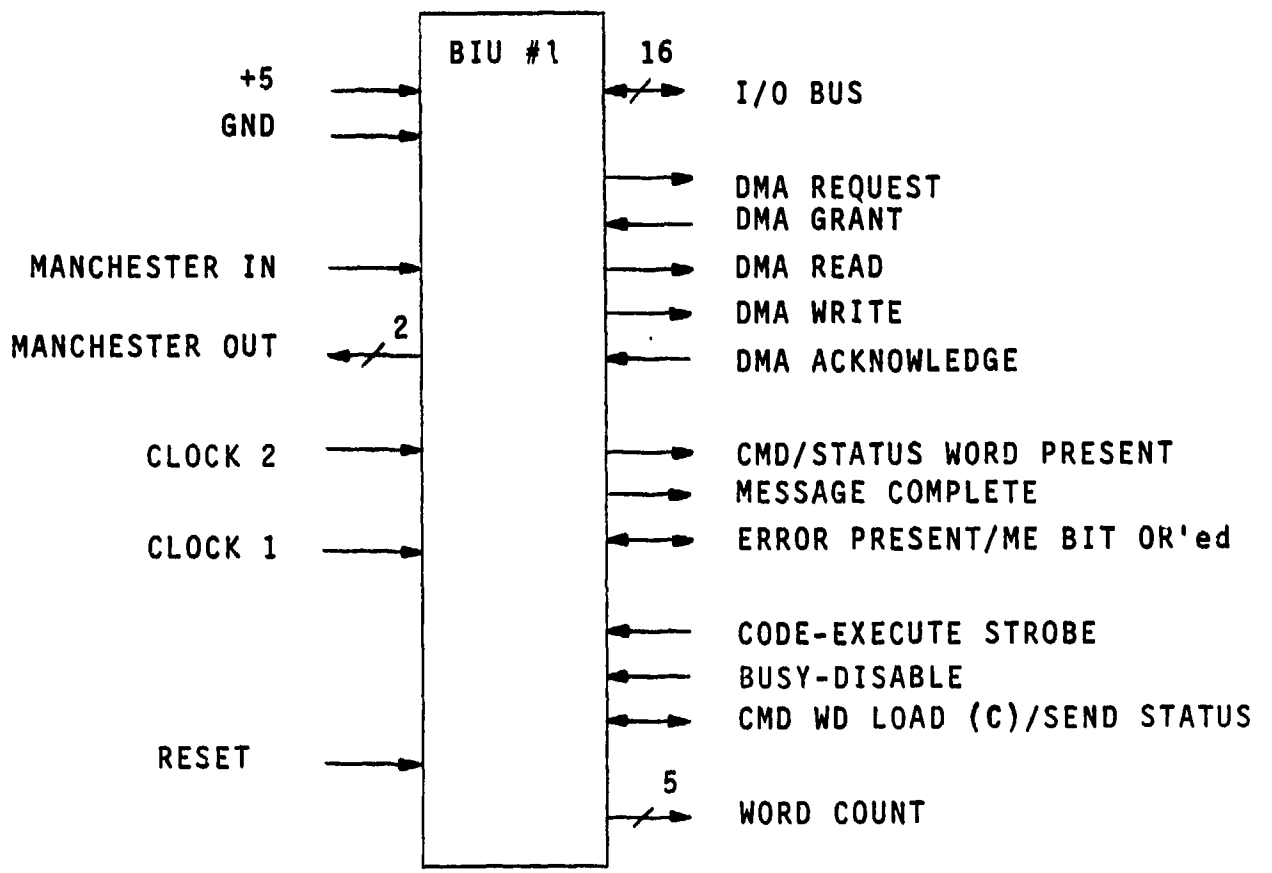

FIGURE 1.1-4
BIU #1 FUNCTIONAL PINOUT

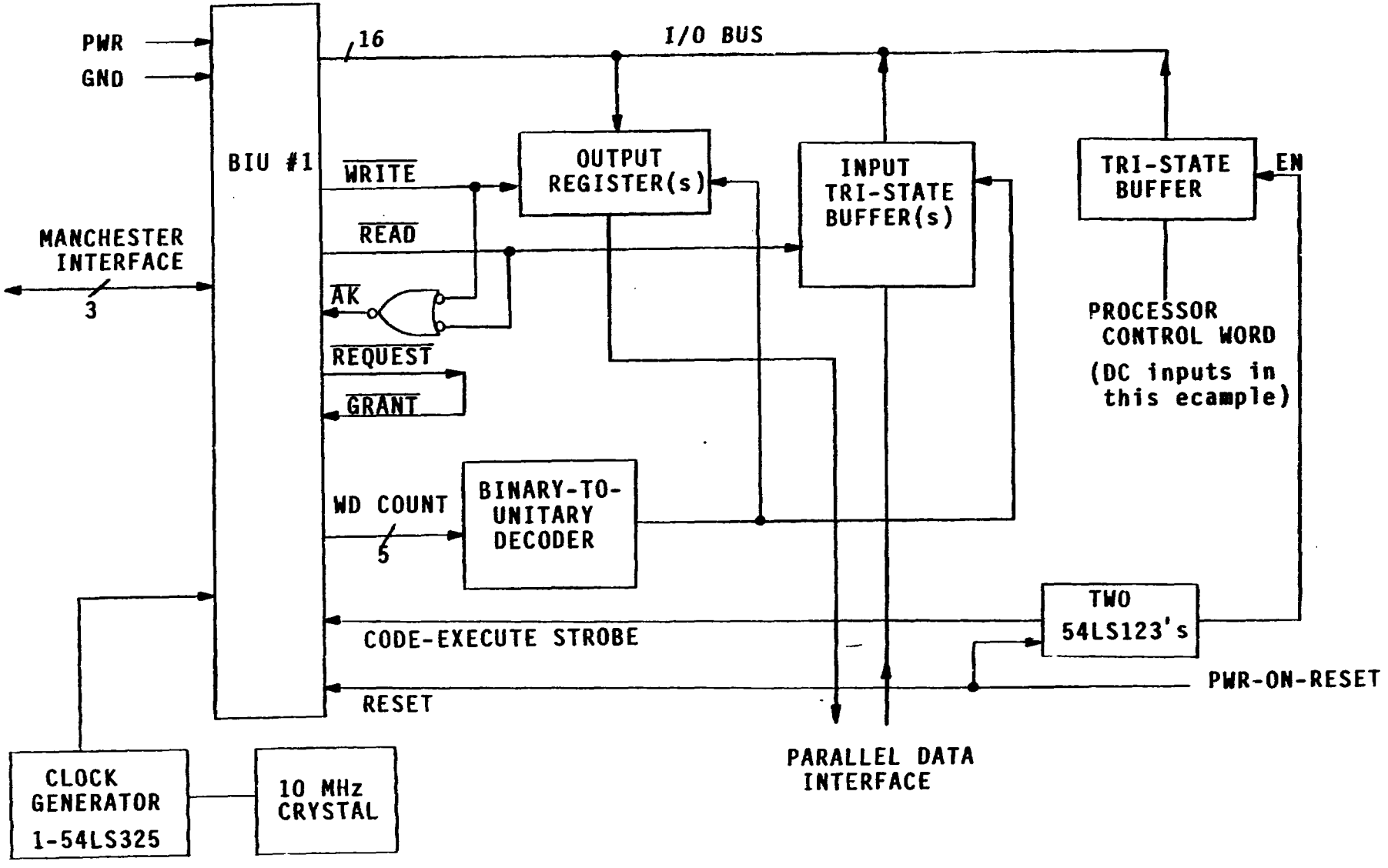

FIGURE 1.1-5
SIMPLE REMOTE TERMINAL

this case, request is fed into the grant input and the OR of write or read is fed into the acknowledge input. Initialization is satisfied by sending the BIU a control word through a separate tri-state buffer. Initialization occurs when the code-execute strobe goes active and 2^0 of the I/O bus is set high. Under these conditions, the BIU treats bits 2^{15} -2^1 in a special way. The control word conveys mode information (8-bit/16-bit and controller/remote), box address, bus-accept status and manchester input configuration control. At power-up, the BIU is reset via the power-on-reset signal. This same signal strobes two of the four single-shots in the two packages of 54LS123's. One of the strobed single-shots enables the processor control word to pass through a set of tri-state buffers to the BIU; the other acts as a delay and then as a trigger to a third single-shot. The third single-shot supplies the code-execute strobe to the BIU and causes it accept the processor control word.

A more general application of Chip #1 without Chip #2 is given in Figure 1.1-6. In that figure, two BIU #1 Chips drive redundant buses on their serial bus side and connect together and to the 8086 I/O bus on their parallel bus side. The data path connection to the 8086 is via a set of bidirectional drivers and a register called the CMD/Status Holding Register.

In the 8086 application, communication occurs via different modes. When the 8086 communicates with the BIU Chips, it treats chip functions as memory mapped I/O's; e.g., a command word loaded into BIU #1A is sent to an address representing that function; a command word loaded into BIU #1B is sent to a different address representing that function; etc. When a BIU communicates with its host, it deposits command words and status words into the CMD/Status Holding Register; these are then available to the 8086 via memory-mapped I/O. Data word communication takes place using DMA. Service by the 8086 is linked through interrupts. A detailed block diagram of a BIU/8086 interface is given in Figure 1.1-7.

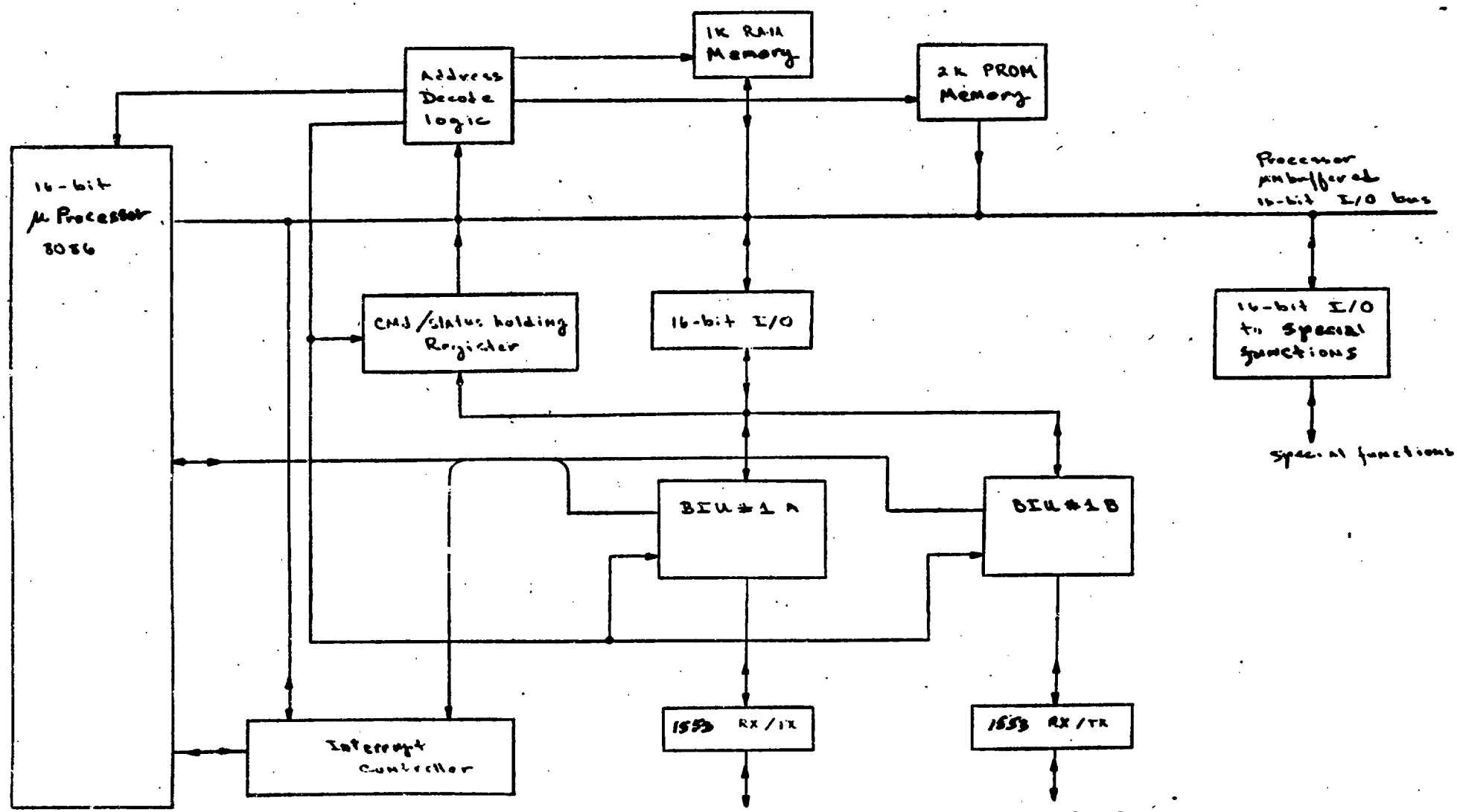

Figure 1.1-6

Interface to 8086-Based μprocessor

BIU #2, as was mentioned above, enhances BIU #1. BIU #2 provides controller capability such that BIU #2 can drive BIU #1 and the two chips thereby implement the bus controller function. BIU #2 contributes the following capabilities:

1) Instruction-fetch via DMA,
2) Message-command-word generation,
3) Data-buffer address generation,
4) Time-tagging of the data stored in host memory by BIU #1,
5) Mode code command execution, and
6) Interrupt generation.

Because of the nature of BIU #2's activities, BIU #2 is basically a register stack with appropriate control logic. A basic block diagram of BIU #2 is given in Figure 1.1-9.

The input and output control lines are split into two groups; those to and from the host, and those to and from BIU #1. The I/O bus is shared and is tied to both host and BIU #1. The basic interconnection between BIU #1, #2, and the host is given in Figure 1.1-10.

When the hardware of Figure 1.1-10 operates in the Master Mode, BIU #2 is set up by the host. The host sends it the instruction address, a base address, and minor cycle time value. It sends both BIU #1 and #2 the processor control word. With these, BIU #2 proceeds to command generation and data buffer address generation. When command generation is completed for a given message, BIU #1 is given the command word(s) and ordered to transmit. BIU #1 deducts whether the message is an RT-transmit or RT-receive message or a mode command and how many words are involved in the transfer. With this information, BIU #1 proceeds with the message implementation and BIU #2 waits for control information. During the actual data transfers, BIU #1 handles the DMA operation. If errors are encountered during the message handling operation, BIU #2 is notified via a discrete control line; the nature of the error is catalogued in BIU #1's error register. Once a message is complete, BIU #2 is notified and it proceeds with appropriate action. If the message involved an error, BIU #2 decides (from information in the instruction words associated with the message) whether a re-try is appropriate and, if not, the error conditions from BIU #1 are moved into BIU #2 and an interrupt generated. If the message is error free, BIU #2 acquires the next instruction words needed to generate the command(s) and data buffer address associated with the next message.

When the hardware of Figure 1.1-10 operates in the Remote Mode, BIU #2 is set up by the host. But, in this mode, BIU #2 only requires the base address word and the control word. BIU #2 still has the task of data buffer address generation. In this situation, BIU #1 signals BIU #2 when a command word for the remote controller has arrived so that BIU #2 will prepare the buffer address. With the address generated, BIU #1 handles all the data transfers by generating the appropriate DMA control signals just as it did in the controller mode.

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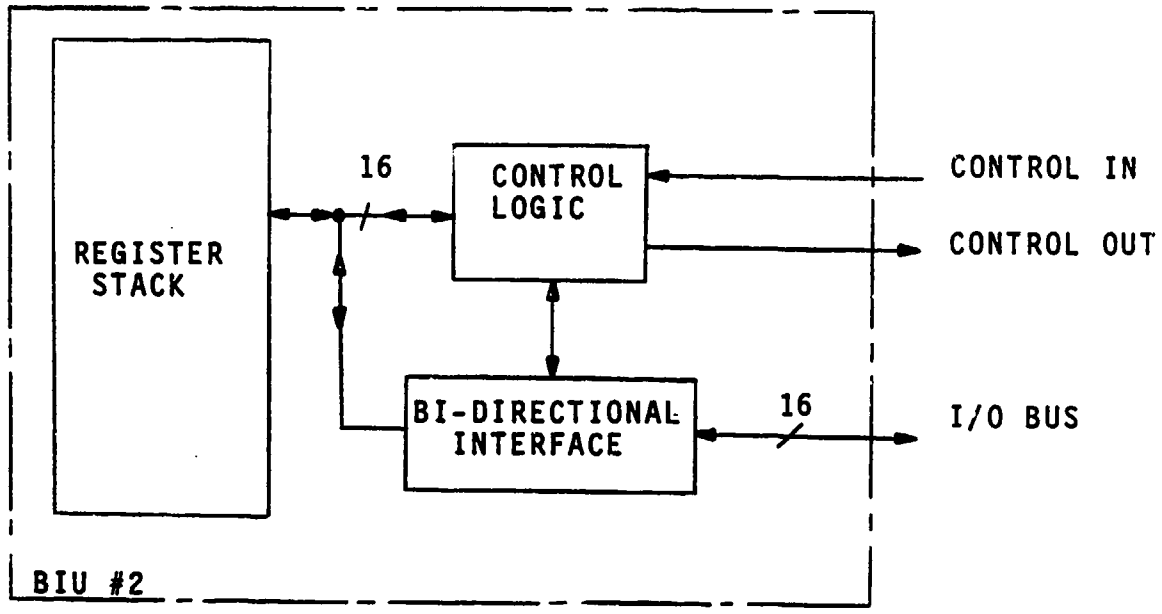


FIGURE 1.1-9
BIU #2 BASIC BLOCK DIAGRAM

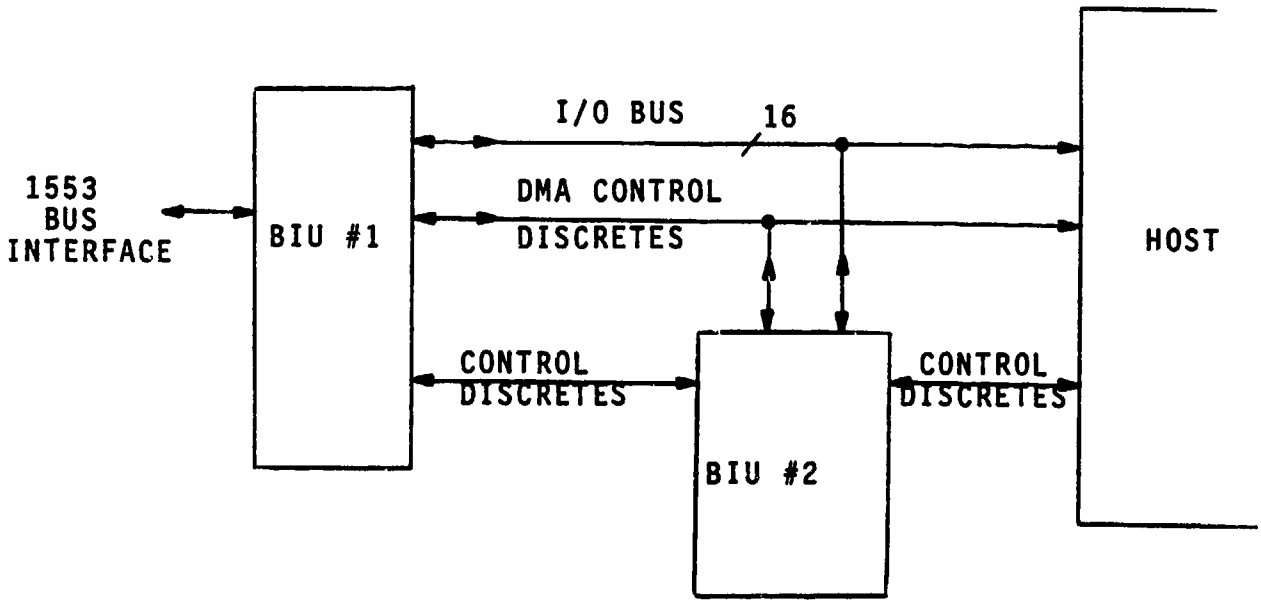


FIGURE 1.1-10
INTERCONNECTION OF BIU #1, #2, AND HOST

The functional pin out of BIU #2 is given in Figure 1.1-11.

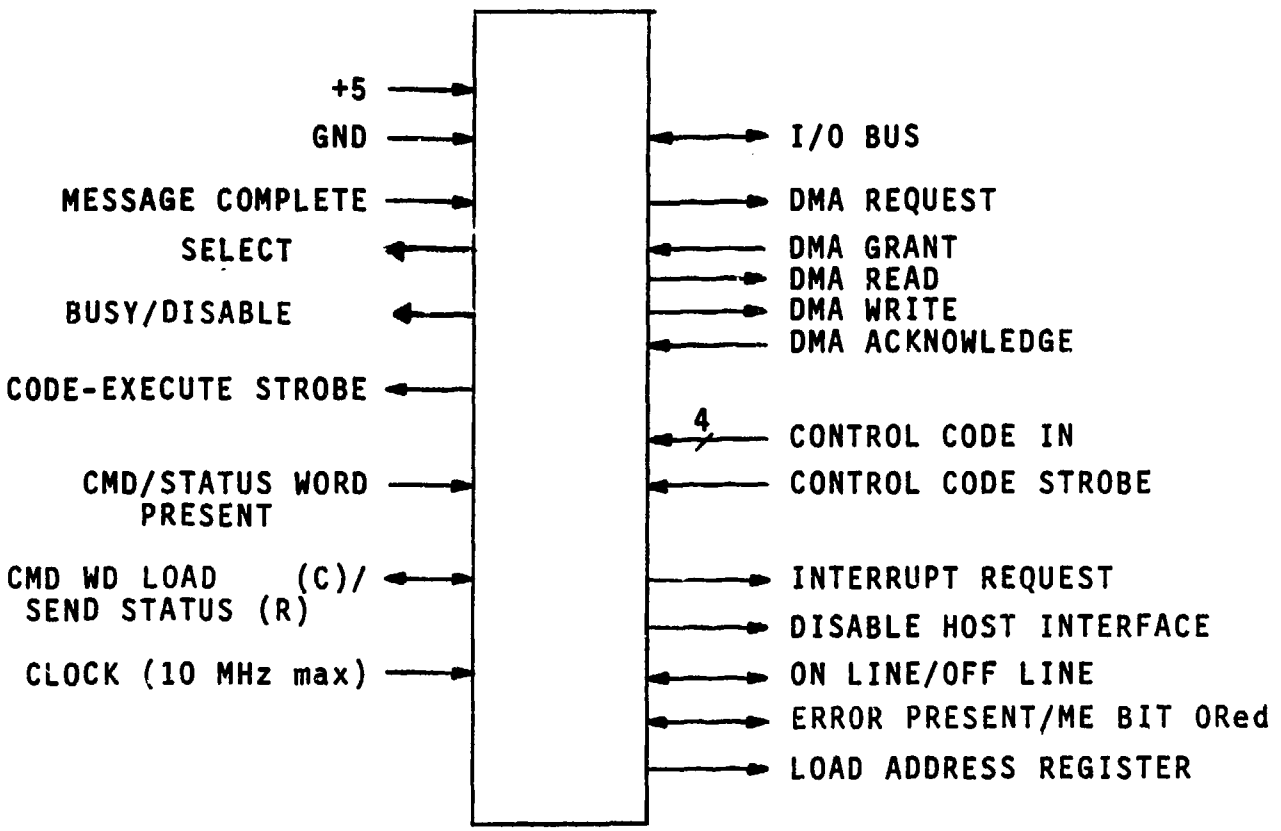


FIGURE 1.1-11
BIU #2 FUNCTIONAL PINOUT

1.2 Detailed Description

This detailed description attempts to supply sufficient information to simplify application of the BIU; it concentrates on the algorithmic aspects of the chips. Following this, section 1.3 supplies a different kind of detail; it concentrates on pin descriptions, timing wave forms etc.

1.2.1 BIU Functional Operation

Back in the general discussion, BIU #1 and #2 were credited with various capabilities. Considering the two chips together, the combined capabilities,

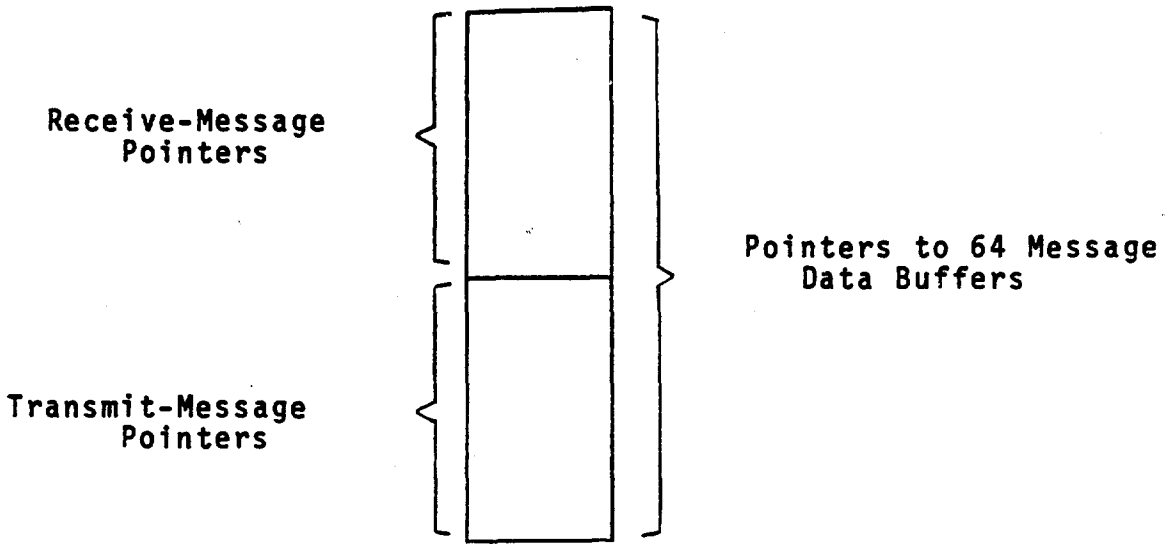
1) instruction fetch via DMA,
2) message command word generation,
3) data buffer address generation,
4) message data handling,
5) time tagging of the data in the data buffers,
6) mode command execution, and
7) interrupt generation, now will be covered in detail.

1.3.1.1 Instruction Fetch and Decode

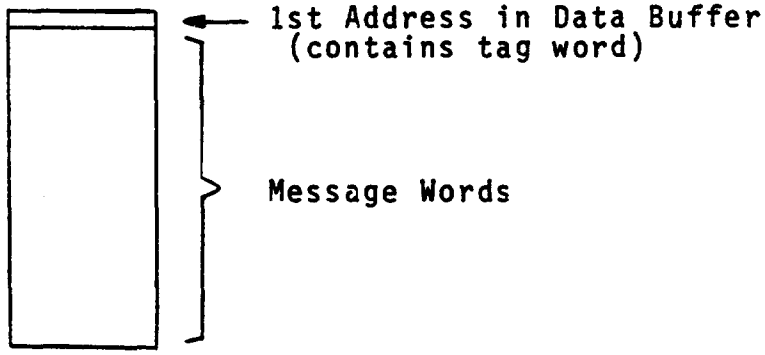
Five major items are covered in this section:

1) data buffer structure,
2) the fetch cycle,
3) command word generation,
4) data buffer address generation, and
5) time tag generation.

The BIU assumes all message data is packed in data buffers accessed indirectly through pointer blocks. Each buffer contains N+1 addresses so a data buffer can hold a tag word and the N message words appropriate to a particular message. The pointer which points to the first address of a given data buffer is to be found in a block of 64 pointers. Any time the BIU reads message words from or writes messages words into host memory, it must first generate the address of the pointer, acquire the pointer and then access the corresponding message-data buffer. To see how this is accomplished, let us look at how the instructions are decoded.



TYPICAL POINTER BLOCK USED BY BIU



TYPICAL MESSAGE-DATA BUFFER

FIGURE 1.2.1.1-1

During initialization the BIU is given data for its Instruction Address Register (IAR) which points the BIU to its stored program. Instructions there are arranged in pairs; the format is given in Figure 1.2.1.1-2. The BIU is also given a Base Address Register (BAR) word; with this and the instruction words it can develop the address into the pointer block and find the data buffer. In a fetch sequence the IAR contents are placed on the 16-bit I/O bus and loaded into an external register. The first of a pair of DMA sequences occurs and the first instruction word is acquired. Again, the IAR contents (internally incremented)are placed on

LSB

1 2	3 4	5	6	7 8 9 10 11	12 13 14 15 16
OP CODE	RE-TRY	B	I	RECEIVE DEVICE ADDRESS	RECEIVE SUBADDRESS/MODE
WORD COUNT/ MODE CODE			S	TRANSMIT DEVICE ADDRESS	TRANSMIT SUBADDRESS/MODE

IW1 BIT	DESIGNATION
1-2	Normal OP Codes Bit 1-2 00 = Halt BIU 01 = Link (Use second word as address of next 2-word instruction) 10 = No Operation (go to next 2-word instruction) 11 = Bus Operation
3-4	Indicates number of retries (0, 1, 2, or 3)
5	0 = Operation is performed on Bus A 1 = Operation is performed on Bus B
6	1 = Interrupt processor upon successful bus operation
7-11	Receive terminal addresses
12-16	00000, 11111 = mode command operation 00001 --- --- 11101 } Receive terminal subaddress 11110 = Asychronous message

IW2 BIT	DESIGNATION
1-5	Word count or mode command code
6	Select = Select Bit 0 = Select Output = "0" Select Bit 1 = Select Output = "1"
7-11	Transmit terminal addresses
12-16	00000, 11111 = mode command operation 00001 --- --- 11101 } Transmit terminal subaddress 11110 = asychronous message

FIGURE 1.2.1.1-2
FORMAT FOR INSTRUCTION WORD PAIR

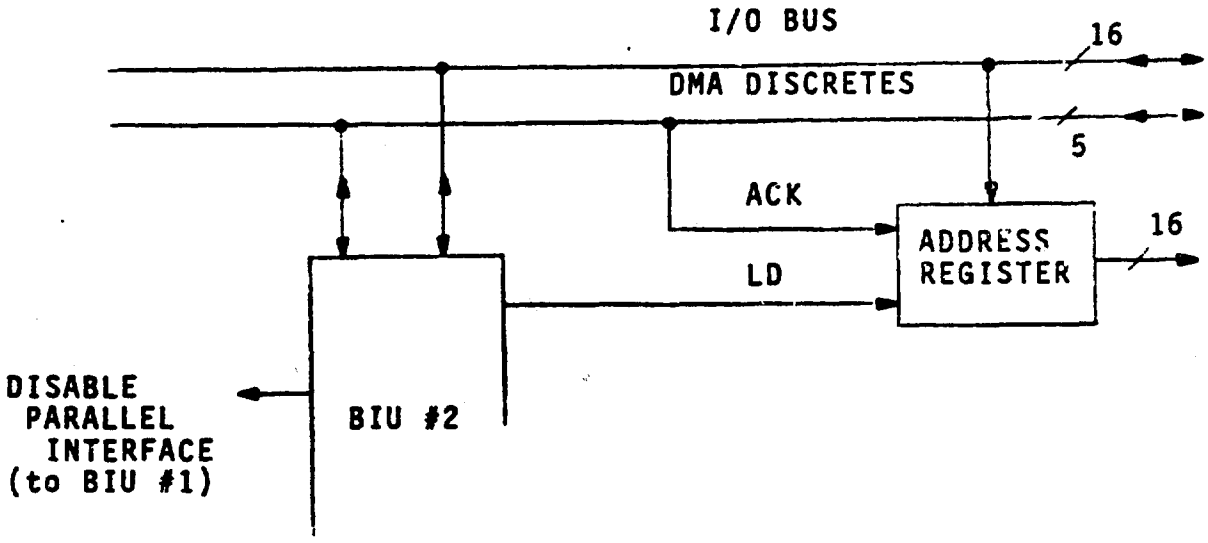


FIGURE 1.2.1.1-3
CONNECTION TO HOST ADDRESS BUS

the 16 bit I/O and loaded into the external register. BIU #2 initiates a second DMA cycle and acquires the second instruction word. (The IAR is incremented again internally to prepare for the next fetch operation).

Once the two instruction words are acquired, BIU#2 can construct the command words. Referring to Figure 1.2.1.1-2 BIU #2 compares its terminal address (available from the control word (PCR word) given to it when setup by the host) with the device addresses in the instruction words. If BIU#2's address is the same as the Receive-Device Address, then the command to be generated is a transmit command to an RT. If BIU #2's address is the same as the Transmit-Device Address, then the command to be generated is a receive command to an RT. If BIU#2's address does not compare with either device address, then an RT-to-RT pair of commands is to be generated. As part of BIT, BIU#2 checks to assure the Receive-Device Address is different from the Transmit-Device Address. (Bit 5 of the Internal Status Word is set when the two are the same.)

When a command is generated, BIU #2 generates a corresponding data buffer address. As mentioned above, BIU #2 is given a Base Address Register (BAR) word. BIU #2 appends six bits (the $\overline{T/R}$ bit and the master's subaddress bits) to the LS end of the BAR word to form an address into a pointer table. The pointer, acquired from the table, points to the first address in the data buffer. This first address is reserved and the pointer to it is stored in the Pointer Register of BIU #2. The incremented value (pointing to the second address of the data buffer) is then loaded into the external address register--ready for use by BIU #1 when it executes its DMA transfers. Once the data buffer address is

set up, BIU #2 is ready to transfer the command word to BIU #1 and command BIU #1 to transmit. From that point, BIU #1 handles the DMA data transfers. If the message is an RT-Receive message, the data transfers by BIU #1 complete the message process. However, if the message is an RT-Transmit message, the data transfers by BIU #1 are followed by a final DMA transfer by BIU #2 of the tag word into the first address of the data buffer. This process is summarized in Figure 1.2.1.1-4.

The discussion above assumed the BIU configured as a controller. In the remote mode, command generation doesn't apply. However, buffer address generation does. This process is summarized in Figure 1.2.1.1-5.

- BIU #2 DMA's instruction words 1, 2 from host.
- BIU #2 compares its terminal address with those in the instruction words.
- When a compare is found, the subaddress/mode field corresponding to that device address constitutes the master's subaddress. When no compare is found, an RT-to-RT message is to be executed and the subaddress used in RT-Receive command of the 2-command sequence constitutes the master's subaddress.
- BIU #2 appends the $\overline{T/R}$ and master's subaddress bits to the LS end of the BAR word to form a 16-bit address into a pointer table:

LSB

BASE ADDRESS (10 bits)	T/R	SUBADDRESS (5 bits)

- BIU #2 DMA's pointer from pointer table; pointer is the location of the first address in the data buffer.
- Pointer is stored in BIU #2's Pointer Register.
- BIU #2 loads incremented value of pointer into external address register.
- BIU #2 generates command word.
- BIU #2 transfers command word to BIU #1.
- BIU #1 handles data DMAs (data storage in RT-RT messages is optional).
- When data is stored in host memory by the BIU, the final data DMA by BIU #1 is followed by a DMA by BIU #2 of the tag word into the first address of the data buffer. The tag word transferred contains the minor cycle number, word count and the data error bit:

LSB

MINOR CYCLE NO. (10 bits)	WORD COUNT (5 bits)	DE

FIGURE 1.2.1.1-4
SUMMARY OF BIU CONTROLLER MODE MESSAGE PROCESSING

- BIU #1 receives an RT-Transmit or an RT-Receive command.
- BIU #1 signals to BIU #2 that a command word is present and passes the command word to BIU #2 via the I/O lines.
- BIU #2 determines the command is an RT-Transmit or an RT-Receive command and begins data buffer address generation.
- BIU #2 appends the T/R and subaddress bits of the command word to the LS end of a 10-bit base address to form a 16-bit address into a pointer table.
- BIU #2 DMA's pointer from pointer table; pointer is the location of the first address in the data buffer.
- Pointer is stored in BIU #2's Pointer Register.
- BIU #2 loads incremented value of pointer into external address register.
- BIU #1 handles data DMAs.
- In the case of an RT-Receive message, the final data DMA by BIU #1 is followed by a DMA by BIU #2 of the tag word into the first address of the data buffer.

FIGURE 1.2.1.1-5
SUMMARY OF BIU REMOTE MODE MESSAGE PROCESSING

1.2.1.2 MODE CODE COMMAND EXECUTION

The mode codes represent commands for action other than the simple transfer of data. Their use is primarly for data and error management. The codes are divided into two groups, those without an associated data word and those with an associated data word. The list of mode commands is given in Table 1. Codes 00000 through 01111 inclusive represent the codes without an associated data word.

TABLE 1

MODE CODES

MODE CODE	MODE COMMAND	T/R BIT
00000	Dynamic Bus Control	1
00001	Synchronize	1
00010	Transmit Status Word	1
00011	Initiate Self Test	1
00100	Transmitter Shutdown	1
00101	Override Transmitter Shutdown	1
00110	Inhibit T/F Flag	1
00111	Override Inhibit T/F Flag	1
01000	Reset Remote Terminal	1
01001	(Reserved)	-
01010	.	.
01011	.	.
01100	.	.
01101	.	.
01110	.	.
01111	(Reserved)	-
10000	Transmit Vector Word	1
10001	Synchronize	0
10010	Transmit Last Command	1
10011	Transmit the BIT Word	1
10100	Selected Transmitter Shutdown	0
10101	Override Selected Transmitter Shutdown	0
10110	(Reserved)	-
.	.	.
.	.	.
11111	(Reserved)	-

The MIL-STD-1553B description of the mode codes is covered in paragraph 1.2.1.2.1. This description is too broad to define BIU operation; so, paragraphs 1.2.1.2.2, 1.2.1.2.3 and 1.2.1.2.4 detail just how the BIU fits within the standard.

Mode codes and the status word are intimately linked, so the status word format and bit descriptions from MIL-STD-1553B are given below.

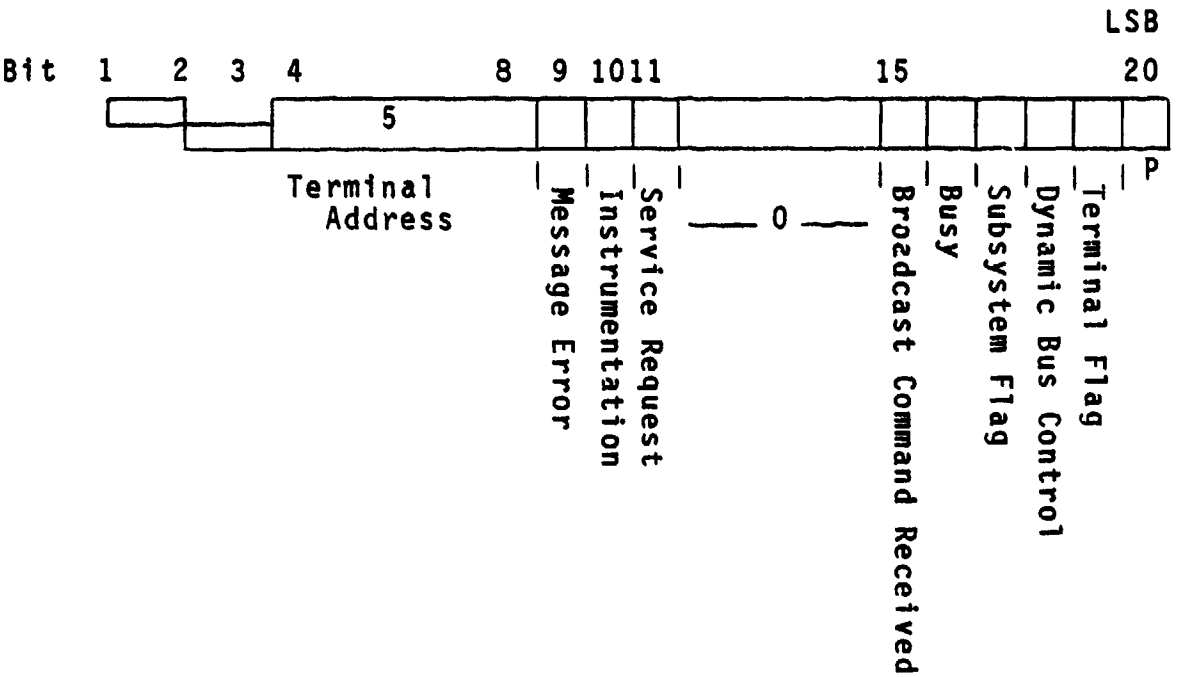


FIGURE 1.2.1.2-1
STATUS WORD FORMAT

SYNC: The sync waveform shall be as specified in Figure 1.2.1.2-1.

RT ADDRESS: The next five bits following the sync shall contain the address of the terminal which is transmitting the status word.

MESSAGE ERROR BIT: The status word bit at bit time nine shall be utilized to indicate that one or more of the data words associated

with the preceding receive command from the bus controller has failed to pass the RT's validity tests. A Logic One shall indicate the presence of a message error, and a Logic Zero shall show its absence. All RTs shall implement the message error bit.

INSTRUMENTATION BIT: Bit time ten of the status word shall be reserved for the instrumentation bit and shall always be a Logic Zero. This bit is used in conjunction with a Logic One in bit time ten of the command word to distinguish between a command word and status word. The use of the instrumentation bit in this manner is optional.

SERVICE REQUEST BIT: The status word bit at bit time eleven shall be reserved for the service request bit. The use of this bit is optional. This bit, when used, shall indicate the need for the bus controller to take specific predefined actions relative to the RT and/or associated subsystem. Multiple subsystems, interfaced to a single RT, which individually require a service request signal shall logically "OR" their individual signals into the single status word bit. In the event this logical "OR" is performed, then the designer must make provisions in a separate data word to identify the specific requesting subsystem. The service request bit is intended to be used only to trigger data transfer operations which take place on an exception rather than periodic basis. A Logic One shall indicate the presence of a service request, and a Logic Zero its absence. If this function is not implemented, the bit shall be set to zero.

RESERVED STATUS BITS: The status word bit times 12 through 14 are reserved and shall not be used. These bits shall be set to a Logic Zero.

BROADCAST COMMAND RECEIVED: The status word bit time of 15 shall be set to a Logic One to indicate that the preceding valid command word was a broadcast command and a Logic Zero shall show its absence. If not used, this bit shall be set to a Logic Zero.

BUSY BIT: The status word bit at bit time sixteen shall be reserved for the busy bit. The use of this bit is optional. This bit, when used, shall indicate that the RT or subsystem

is unable to move data to or from the subsystem in compliance with the bus controller's command. A Logic One shall indicate the presence of a busy condition, and a Logic Zero its absence. In the event the busy bit is set in response to a transmit command, then the RT shall transmit its status word only. If this function is not implemented, the bit shall be set to Logic Zero.

SUBSYSTEM FLAG BIT: The status word bit at bit time seventeen shall be reserved for the subsystem flag bit. The use of this bit is optional. This bit, when used, shall flag a subsystem fault condition, and alert the bus controller to potentially invalid data. Multiple subsystems, interfaced to a single RT, which individually require a subsystem flag bit signal, shall logically "OR" their individual signals into the single status word bit. In the event this logical "OR" is performed, then the designer must make provisions in a separate data word to identify the specific reporting subsystem. A Logic One shall indicate the presence of the flag, and a Logic Zero its absence. If not used, this bit shall be set to Logic Zero.

DYNAMIC BUS CONTROL ACCEPTANCE BIT: The status word bit at bit time eighteen shall be reserved for the acceptance of dynamic bus control. The use of this bit is optional. This bit, when used, shall indicate acceptance or rejection of a dynamic bus control offer. A Logic One shall indicate acceptance of control, and a Logic Zero shall indicate rejection of control. If this function is not used, this bit shall be set to Logic Zero.

TERMINAL FLAG BIT: The status word bit at bit time nineteen shall be reserved for the terminal flag function. The use of this bit is optional. This bit, when used, shall flag an RT fault condition. A Logic One shall indicate the presence of the flag, and a Logic Zero, its absence. If not used, this bit shall be set to Logic Zero.

PARITY BIT: The least significant bit in the status word shall be utilized to indicate odd parity of the status word.

1.2.1.2.1 MODE COMMANDS AS PER 1553B

The following command descriptions are from MIL-STD-1553B.

DYNAMIC BUS CONTROL: The controller shall issue the mode command to an RT capable of performing the bus control function. This RT shall respond with a status word. Control of the data bus passes from the offering bus controller to the accepting RT upon transmission of the status word by the RT. If the RT rejects control of the data bus, the offering bus controller retains control of the data bus.

SYNCHRONIZE: This command shall cause the RT to synchronize; e.g., reset timer, start sequencer, etc. The RT shall respond with the status word.

TRANSMIT STATUS WORD: This command shall cause the RT to transmit the status word associated with the last valid command word. This mode command shall not alter the state of the status word.

INITIATE SELF TEST: This command shall be used to initiate self test within the RT. The RT shall respond with the status word.

TRANSMITTER SHUTDOWN: This command (to only be used with dual redundant bus systems) shall cause the RT to disable the transmitter associated with the redundant bus. The RT shall not comply with a command to shut down a transmitter on the bus from which this command is received. In all cases, the RT shall respond with a status word.

OVERRIDE TRANSMITTER SHUTDOWN: This command (to only be used with dual redundant bus systems) shall cause the RT to enable a transmitter which was previously disabled. The RT shall not comply with a command to enable a transmitter on the bus from which this command is received. In all cases, the RT shall respond with a status word.

INHIBIT T/F FLAG: This command shall cause the RT to set the T/F Flag bit in the status word to Logic Zero until otherwise commanded. The RT shall respond with the status word.

OVERRIDE INHIBIT T/F FLAG: This command shall cause the RT to override the inhibit T/F flag mode command control. The RT shall respond with the status word.

RESET REMOTE TERMINAL: This command shall be used to reset the RT to a power-up initialized state. The RT shall first transmit its status word, and then reset.

RESERVED MODE CODES (01010 to 01111): These mode codes are reserved for future use and shall not be used.

TRANSMIT VECTOR WORD: This command shall cause the RT to respond with a status word and a data word containing service request information.

SYNCHRONIZE (WITH DATA WORD): The RT shall receive a command word followed by a data word. The data word shall contain synchronization information for the RT. After receiving the command and data word, the RT shall transmit the status word.

TRANSMIT LAST COMMAND WORD: This command shall cause the RT to transmit its status word followed by a single data word which contains bits 4-19 of the last command word, excluding a transmit last command word mode code received by the RT. This mode command shall not alter the state of the RT's status word.

TRANSMIT BUILT-IN-TEST (BIT) WORD: This command shall cause the RT to transmit its status word followed by a single data word containing the RT BIT data. This function is intended to supplement the available bits in the status word when the RT hardware is sufficiently complex to warrant its use. The data word, containing the RT BIT data, shall not be altered by the reception of a transmit last command or a transmit status word mode code. This function shall not be used to convey BIT data from the associated subsystem(s).

SELECTED TRANSMITTER SHUTDOWN: This command shall cause the RT to disable the transmitter associated with a specified redundant data bus. The command is designed for use with systems employing

more than two redundant buses. The transmitter that is to be disabled shall be identified in the data word following the command word. The RT shall not comply with a command to shut down a transmitter on the bus from which this command is received. In all cases, the RT shall respond with a status word.

OVERRIDE SELECTED TRANSMITTER SHUTDOWN: This command shall cause the RT to enable a transmitter which was previously disabled. The command is designed for use with systems employing more than two redundant buses. The transmitter that is to be enabled shall be identified in the data word following the command word. The RT shall not comply with a command to enable a transmitter on the bus from which this command is received. In all cases, the RT shall respond with a status word.

RESERVED MODE CODES (10110 to 11111): These mode codes are reserved for future use and shall not be used.

1.2.1.2.2 MODE COMMANDS IMPLEMENTED BY THE BIU

BIU #1 implements some of the mode codes without help from the most. These include:

00000	Dynamic Bus Control
00010	Transmit Status Word
00110	Inhibit T/F Flag
00111	Override Inhibit T/F Flag
10010	Transmit Last Command

Mode Command 00000 is implemented by returning the status word with the accept bit set if the remote accepts bus mastership. BIU #1 contains a control register in which the accept bit is held. Initialization by the remote host includes setting or not setting the accept bit. Reception of a 00000 mode command causes BIU #1 to gate the accept bit from the control register into the status word sent in reply to the master. All mode commands are fed back to the host for any desired additional reaction; in the 00000 case, the host would note the offer and take appropriate follow up action if required.

In implementing 00010, BIU #1 simply transmits the contents of the internal status word register to the controller. Mode commands, Transmit and Status Word, and Transmit the Command Word do not affect the contents of the status word.

Mode Command 00110 is implemented in BIU #1 by forcing the T/F flag to remain at Logic Zero; Mode Command 00111 removes the forced inhibit set by Mode Command 00110 and enables the T/F flag to reflect BIU #1 handshake failure, BIU #1 loop test failure, transmitter shutdown mode code, and any RT failure supplied from outside the BIU via the BIT word.

To implement Code 10010, BIU #1 first transmits the contents of the status word register and then transmits the contents of the last command word register back to the controller. The command word, Transmit Last command, does not get loaded into the last command register. Any other valid command for the RT is loaded into the last command word register.

BIU #1 and BIU #2, working together, implement the following mode commands:

00001	Synchronize
10000	Transmit Vector Word
10001	Synchronize (with data word)
10011	Transmit the BIT Word

Before describing the operations implementing these mode commands, note that BIU #2 contains the following registers as part of its register stack:

BIT Word Register	(BIT)
Mode Data Register	(MDR)
Internal Status Register	(ISR)
Master Function Register	(MFR)

BIT holds the particular message failures and terminal failures; and hence, represents the next level of failure detail beyond the single bit representations (the ME and T/F bits) found in the message status word. MDR holds mode data; it holds the data word received with a mode command or the data word to be transmitted with a mode command. (One exception in loading mode data exists. This is explained as part of the description of the Synchronize command used with the MFR.) The ISR typically holds the conditions which indicate the reason an interrupt to the host was last generated.

The mode commands above operate on these four registers. Code 00001 received by the BIU causes BIU #2 to set the System Interrupt Bit (bit 5) in the Internal-Status register and then interrupt the host.

Code 10011 received by the remote BIU causes BIU #2 to pass the BIT word to BIU #1 for transmission (after the status word) back to the controller; the controller's BIU #1 passes the received BIT word to BIU #2. BIU #2 stores this word in its MDR. BIU #2 then sets bit 6 of the ISR (indicating mode data is present) and generates an interrupt. BIU #2 resets the BIT word upon reception of all valid command words for the RT except for the Transmit Status Word, Transmit Last Command, and Transmit BIT Word mode commands.

Code 10001 received by the Remote BIU causes BIU #1 to pass the minor cycle count (used in tag word generation) to BIU #2. BIU #2 stores this in its MFR, sets bit 9 in its ISR (indicating minor cycle data is present) and generates an interrupt. Generation of this mode command by the controller requires its BIU #2 to pass the minor cycle count from its MFR to BIU #1 for transmission following the mode 10001 command word.

Code 10000 received by the Remote BIU causes its BIU #2 to transfer the contents of its MDR to its BIU #1 for transmission after the status word back to the controller. At the controller's BIU, the mode data word is handled as in Code 10011 above. This mode command, requesting the vector word, is the controller's typical response to the Service Request (SR) or Subsystem Flag (SF) bit set in the RT status word. The 16 Vector Bits are loaded into the MDR by the RT host via BIU #2 Control Code 0000. The SR and SF

bits are also loaded into two flag flip-flops in BIU #2 via BIU #2 Control Code 0101. Each time BIU #1 is to send the status word, the SR and SF flags are transferred from BIU #2 into the status word in BIU #1. The master controller, receiving the status word, recognizes the SR or SF bit set and generates an interrupt. The interrupted host, determining the interrupt cause, requests the vector word. When the Transmit Vector Word mode command is received by the RT, BIU #2 uses the detection of the command as a reset signal for the SR and SF flag flip-flops and returns the 16 bit vector contained in the MDR. Note that resetting the SR and SF flag flip-flops has no affect on the contents of the MDR. So, message errors should not affect the eventual acquisition of the vector word through automatic retrys.

1.2.1.2.3 Mode Commands Implemented Outside the BIU

Several mode commands are passed on to the host for implementation. In the group without associated data word these are:

00011 Initiate Self Test
00100 Transmitter Shutdown
00101 Override Transmitter Shutdown
01000 Reset Remote Terminal

The Transmitter-Shutdown command sets the Other-Bus-Inoperative bit in BIU #2's BIT word. The Override-Transmitter-Shutdown command resets that bit; the Other-Bus-Inoperative bit is also controllable by the RT host (see para 1.2.1.2.4). The actual control of the transmitters is implemented externally.

Typically, BIU #1 indicates when the mode codes are to be examined and supplies the command word lines necessary for code detection. The implementation of these code detectors and the subsequent control logic is left to the user. The same comment applies to the reserved mode codes without data word.

Mode commands with data word which rely mostly on host implementation are:

10100 Selected Transmitter Shutdown
10101 Override Selected Transmitter Shutdown

These and the reserved mode codes with an associated data word are partially implemented by the BIU. If a host instructs a controller BIU to send one of these and it is a receive-mode command, the controller will send the command followed by the word it finds in its MDR. The remote, receiving the command, will store the associated data word in its MDR. The process is reversed for a transmit-mode command:

1) the remote receiving the transmit command returns the status followed by data from its MDR,

and, 2) the controller collects the data word in its MDR.

The BIU which stores the received data word in its MDR sets bit 6 in its ISR and interrupts its host.

1.2.1.2.4 Status Word Control

Except for mode commands

1) Transmit the Status Word, and
2) Transmit the Command Word,

the status word is updated upon reception of a valid command word. The bits affected:

1) Message Error,
2) Service Request,
3) Broadcast Command Received,
4) Subsystem Flag, and
5) Terminal Fail Flag.

Of all the status bits, the Broadcast Command Received Bit is the least complicated. So, let it be dispensed with first.

Broadcast Command Received is set when BIU #1 detects a valid broadcast message. Since the status word is suppressed when a broadcast message is received and the Broadcast-Command-Received bit is reset upon reception of a valid command, the controller can only assure that an RT has successfully received a broadcast message by sending a Transmit-The-Status-Word or transmit-last-command mode command to the desired RT following the broadcast message.

The status bits,

1) Message Error,
2) Service Request,
3) Subsystem Flag, and
4) Terminal Fail Flag,

require consideration from several aspects. First of all, note that the Service Request and Subsystem Flag are only influenced by Chip #2; the other two bits can reflect either Chip #1 of #2. Also note that BIU #1 collects status on these bits from Chip #2 at the front end of each message for the RT.

The collection by BIU #1 goes as follows. BIU #1 always activates its Send-Status discrete to BIU #2 upon detection of one of its command words. As the RT's command word is being shifted into its decoder, the ID check is passed and BIU #1 requests BIU #2 to send the Service Request, Subsystem Flag and Terminal-Fail bits. After about 5 bit times, the Send-Status discrete is deactivated and the status data on the I/O lines is saved by BIU #1 in a buffer register. The fourth status bit, Message Error, is collected from BIU #2 differently and a little later. Following the send-status scenario, BIU #1 begins the command word transfer to BIU #2. In the 16-bit mode (the only mode Chip #1 and #2 operate in jointly), BIU #1

sets the newly arrived command word out on its I/O for 4 bit times. After 1½ bit times, BIU #1 activates the Command-Word-Ready discrete to Chip #1 and holds it active low for 1½ bit times. During this sequence, the Error-Present discrete is tri-stated from Chip #1. During the time Command-Word-Ready is active, Chip #2 activates the Error-Present discrete with its Message Error data. On the trailing edge of Command-Word-Ready, BIU #1 saves the ME bit sent to it by BIU #2. With that, BIU #1 completes acquisition of status from BIU #2. (Note that the states of the Service Request and Subsystem Flag bits in Chip #2 are not affected by this transfer process. See Paragraph 1.2.1.2.2 for an explanation of their reset procedure).

As stated above, BIU #1 collects some status bits early; only the terminal ID field is examined when a decision is made tc fetch status bits from BIU #2. If the command received is the Transmit Status Word or Transmit The Last Command Word mode command, then the three bits collected in anticipation are ignored and the fourth to be loaded into the status register at the trailing edge of Command Word Ready is not clocked.

Within Chip #1, the message errors are ORed as shown in Figure 1.2.1.2.4-1. The error bits are held in flip flops. When the BIU #1 pulse, Command Word Ready, is not disabled by the arrival of one of the two special mode codes above, it clocks BIU #2's ME bit into a storage FF in BIU #1, transfers the three status bits obtained earlier into status register flip flops and clears the BIU #1 message error holding flip flops. Regarding the latter, the only other conditions which clear the error flip flops are Power-On-Reset and Processor Control Register (PCR) word load.

Within Chip #1, the Terminal Fail flags are ORed as shown in Figure 1.2.1.2.4-2. The TF flags are treated just like the message error bits. The two TF bits in Chip #1 even have identical reset conditions. Only the fact that two separate failure classes are represented by the individual errors requires that there be separate logic circuits.

Before continuing this description of status word control, some background leading to the tactics used above might prove informative. First of all, the anticipatory transfer of the three status bits is made to spread out in time the inter-chip activity that occurs during the beginning of a message. Prior to command word transfer the I/O bus is available; hence, the transfer of the three bits. The ME bit presents a special problem in that the ME contribution from BIU #2 reflects error conditions determined by the host. The host can use BIU signals together with external logic to check the commands sent to the RT. The RT may be unable to handle commands with certain subaddresses or mode commands with certain mode codes, etc., and, for the specific RT, these commands would be deemed illegal. The discrete input, ME bit in, of BIU #2 facilitates setting the ME bit upon detection of an illegal command. During the command word's presence on the I/O, the external logic checks the

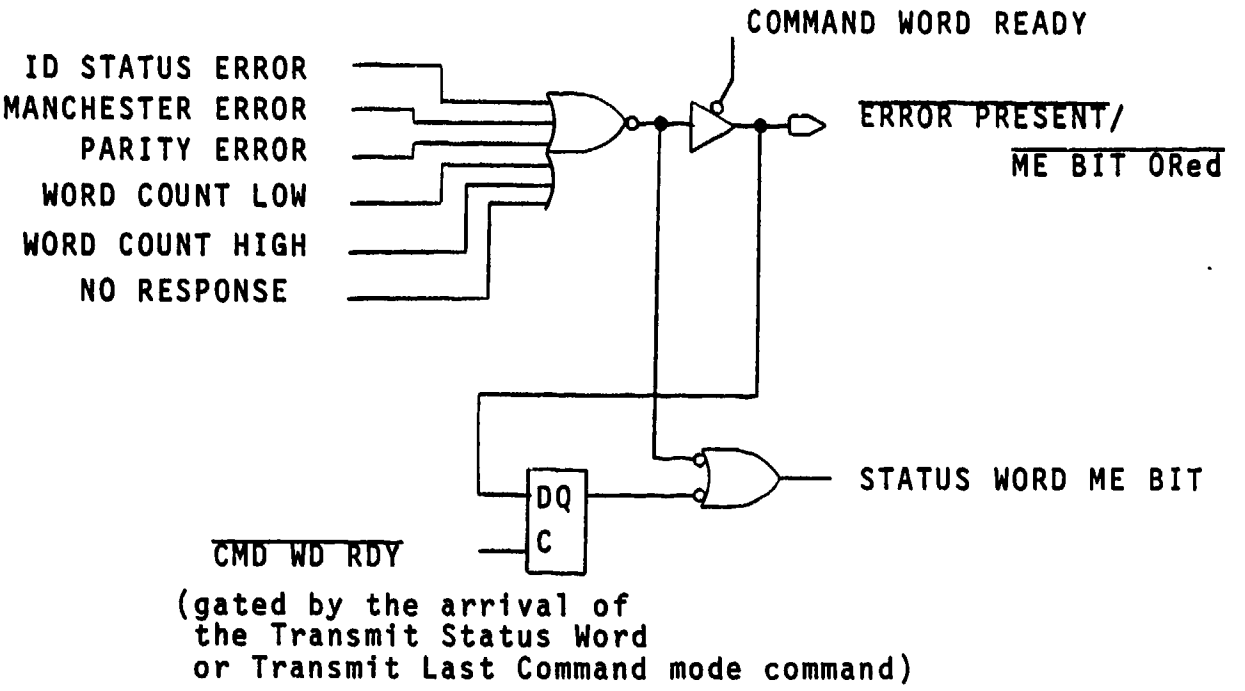


FIGURE 1.2.1.2.4-1
ME BIT ORed CIRCUIT

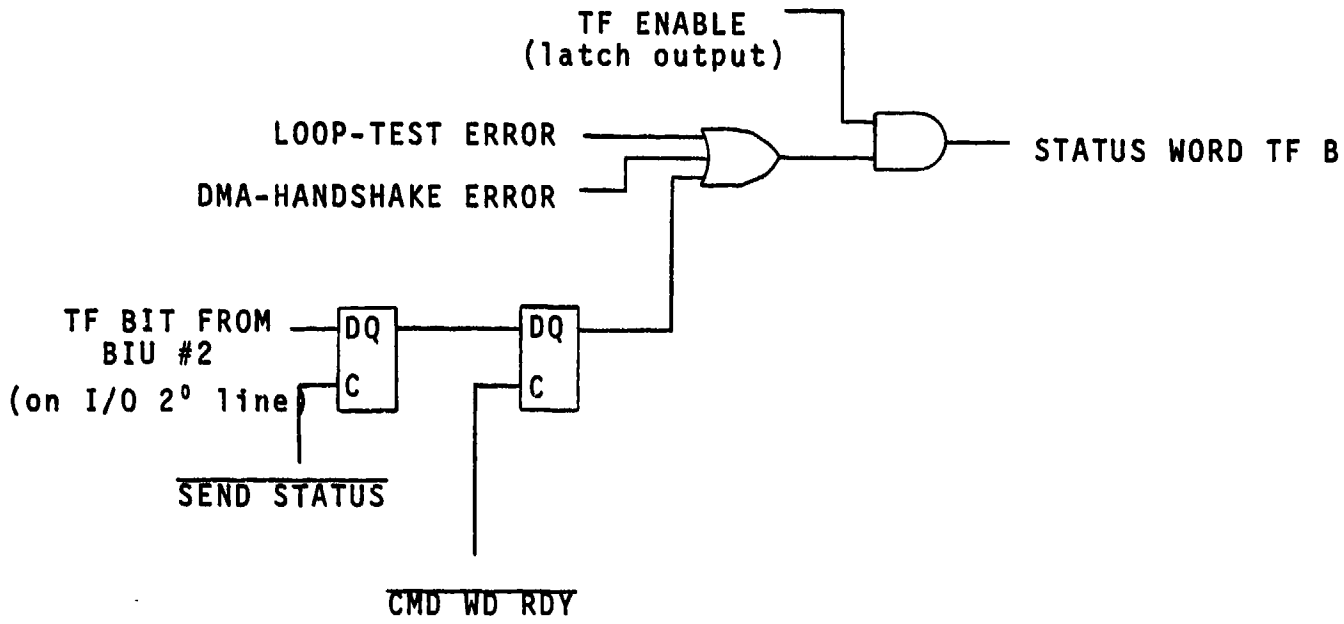


FIGURE 1.2.1.2.4-2
TF BIT ORed CIRCUIT

command word aspects of interest and propagates the checker's output into the input of BIU #2. This result passes through BIU #2 and into BIU #1 via the Error Present/ME Bit ORed discrete as described above. Since this check is valid only toward the latter part of the time the command is present on the inter-chip I/O bus, ME from Chip #2 is sampled as above.

As a point of philosophy, the message errors detected by RT BIU #1 during an RT-receive message cause BIU #1 to suppress the status word; BIU #1 OR's the detected errors into the ME bit of the status word but no status word is returned. Some error conditions, e.g., word count errors, invite bus crashes if the status word is returned. The BIU does not attempt to sort and respond to some errant messages but simply withholds the status word on all errant, RT-receive messages. With this arrangement, the master controller sends the RT-receive message; then, because the message is errant and no status word is returned, the controller notes the "no-response" and typically retrys the message. If retrys fail, the controller typically uses the mode commands to retrieve the status word, BIT word, etc., to be used in a recovery procedure. With this process in mind, the ME bit set in the status response to an RT-receive message will only reflect BIU #2's contribution to the ME bit. Regarding an RT-transmit message, the ME bit set in the status response will again only reflect BIU #2's contribution. The command word must be valid (free of message errors and containing the correct terminal address) before BIU #1 will respond to it. So, the ME bit set in the returned status word cannot represent invalid manchester, etc. Contributions to the ME bit from BIU#1 and #2 would occur jointly when the discrete input to BIU #2 was set and BIU #1 detected a message error.

The Terminal Fail (T/F) bit, as mentioned above, can reflect BIU #1 or BIU #2 inputs, or both. BIU #1 OR's its internal loop test and its DMA-handshake test into the T/F bit. A loop test failure indicates that BIU #1 was unable to successfully compare data input to its encoder in parallel form with data passed through the encoder, transmitter, receiver, and collected by its decoder. A DMA-handshake failure indicates that BIU #1 was unable to complete the DMA-handshake before it was required (by its decoder or encoder) to pass another data word between itself and the host. BIU #2 OR's seven bits (Power-On-Reset, External-Terminal-Fail, and Other-Bus-Inoperative) from its BIT word into the T/F bit. Six of these bits, External-Terminal-Fail and Other-Bus-Inoperative, can be set or reset by the RT host via BIU #2 control code 0110, Load Bit Register bits. The External-Terminal-Fail BITS is controlled only by the host. The Other-Bus-Inoperative bit can be set by the Transmitter-Shutdown mode command and can be reset by the Override-Transmitter-Shutdown mode command besides being controlled by the host. The third bit, Power-On-Reset, is set when the BIU #2 internal voltage level detector indicates an initialization or power dropout has occurred.

1.2.1.3 Interrupt Generation

As mentioned above, the BIU sets interrupts on various conditions, including:

1) message errors,
2) status word exceptions,
3) certain mode commands,
and, 4) program requirements.

Interrupt generation reflects one of several facts:

1) The BIU has encountered a manchester bus data transfer problem and error indications cannot be overcome without host intervention,

or, 2) The BIU has been initialized because of a power dropout or startup and needs to be set up by the host,

or, 3) The BIU has finished the bus oriented tasks required of it by the BIU program in host memory and the program requires host notification,

or, 4) The host decides to intervene in BIU operation and commands the BIU to gracefully halt operation.

As the word itself indicates, an interrupt is a break in an on-going operational scenario, and when such a break occurs, some trace of what happened must be recorded. Here the possible reasons for interrupt generation are recorded by the BIU in BIU #2's Internal Status Register (ISR) and Bit Register (BIT). Both of these are available to the BIU host and BIT in a remote controller is available to the master controller via the manchester bus by use of a mode command.

These interrupts can be viewed from two perspectives, that of the master controller and the remote terminal. These aspects are covered below.

1.2.1.3.1 Interrupts Generated in the Master Controller

Message errors detected by the BIU include:

1) manchester bi-phase errors,
2) word parity errors,
3) no response,
4) message too short, and
5) message too long.

The BIU may diagnose a message error incorrectly to begin with. For example, an error could be of such a nature that the sync detection conditions of the last data word of a given message were distorted and the BIU, not detecting the last word, registers an error of message-too-short. The BIU has automatic-retry capability and can be programmed for up to three additional message communication attempts. So, hard failures tend to be separated from random error occurances suggested by this example.

In the case of a hard failure, the BIU will exhaust the retry attempt(s) and still find that message errors are present. When the BIU executes a message sequence, BIU #1 signals the failure of the sequence via the Error-Present line to BIU #2. At the end of message execution, the Error-Present flag prompts BIU #2 to transfer the error word data (representing specific message errors, Power-On-Reset, DMA error and the Loop-Test error) from BIU #1 into its BIT word (see Figure 1.2.1.3.1-1). BIT is cleared each time the BIU prepares to communicate on the bus. If BIU #1 indicates errors and the retry count is zero, BIU #2 will interrupt the host and halt its operation.

For the moment, set aside the discussion above and consider the treatment given to status words by the master controller. In each of the typical data bus messages, BIU #1 signals BIU #2 when a status word is present. BIU #2 uses the signal to load the incoming status word into the Recv Status Word Register (RSWR) or the Xmit Status Word Register (XSWR). Which status word goes to which register is indicated by Figure 1.2.1.3.1-3. BIU #2 selects the SWR to be loaded by way of information made available during the command word generation process. This SWR-Select signal is also used with the Status-Word-Present and the Error-Present signals from BIU #1, together with status word contents, to set status-word-related bits 10 thru 13 of BIU #2's ISR register. Setting bit 12 or 13 indicates the status word contained a parity, address or manchester error.

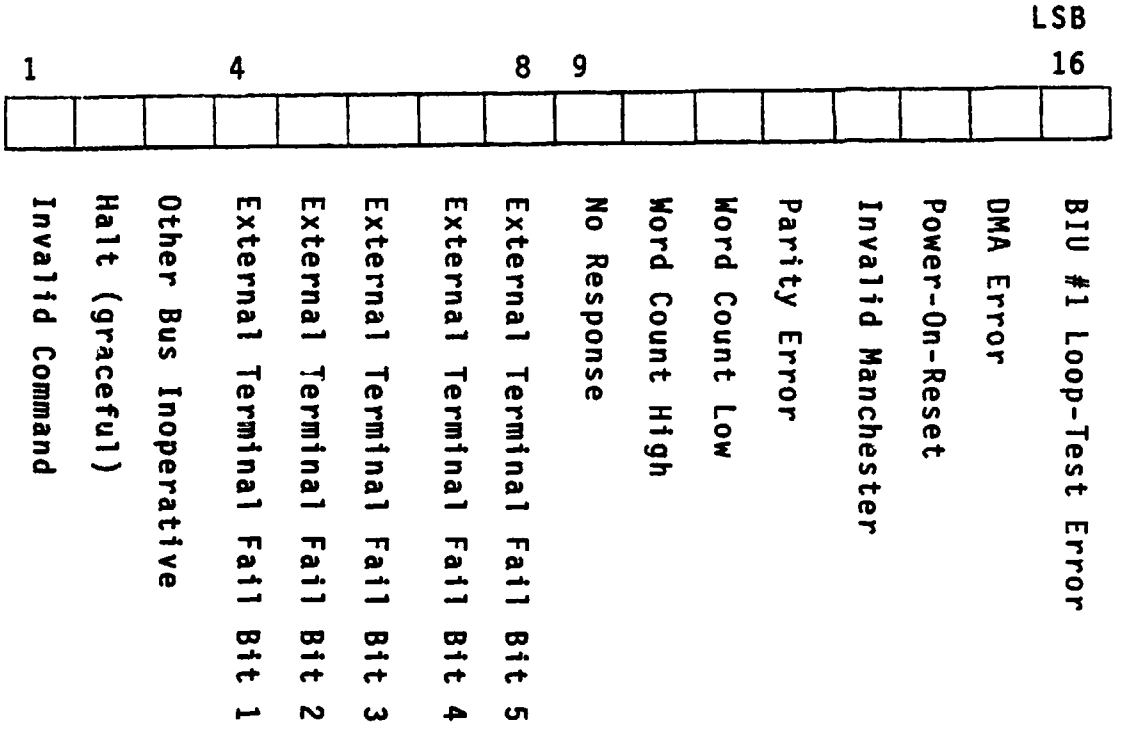


FIGURE 1.2.1.3.1-1
BIT WORD FORMAT

FIGURE 1.2.1.3.1-2
INTERNAL STATUS REGISTER (ISR)

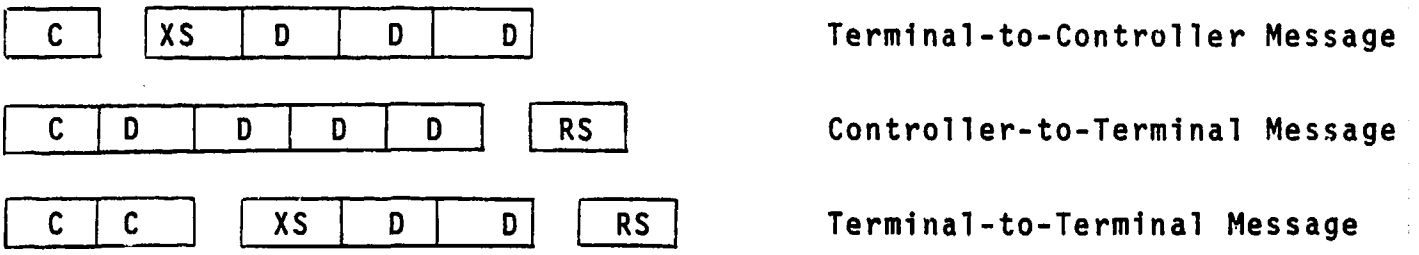


FIGURE 1.2.1.3.1-3
TYPICAL DATA BUS MESSAGES

As far as retry attempts are concerned, the Error-Present flag will prompt the BIU to either rectify the error in the status word or cause an interrupt to be generated. Setting bits 10 or 11 of the ISR register indicates the status word was valid but contained some "exception" (ME, T/F, Service Request, etc., see Figure 1.2.1.3.1-1). For this situation, the Error-Present flag would not be set and, hence, would not prompt BIU #2 to initiate a retry attempt. Yet, two status word exceptions (ME, Subsystem Busy = 1) indicate the Receive Command just transmitted was unsuccessfully received by the terminal and that a retry might rectify the problem. So, like the Error-Present flag, the two exceptional conditions found in the valid status word prompt BIU #2 to test the retry count and either execute another message sequence or generate an interrupt.

Beside generating interrupts when message error or busy conditions prevent successful communications, BIU #2, as part of the master controller configuration, generates interrupts in response to other conditions described below. In these cases, the BIU always stops operation until the interrupt is properly serviced.

Under two conditions BIU #2 will generate an interrupt when programmed to do so. The instruction pair used for command generation contains a 1-bit field (see Figure 1.2.1.1-2) which, when set, requires the BIU to generate an interrupt after executing any other action required by the instruction pair. The instruction pair may require a bus operation and, during execution, the controller may detect a message error or status word exception, ME or Subsystem Busy = 1. Under any of these conditions, programmed message retrys are attempted before generating the programmed interrupt. If the bus operation is ultimately unsuccessful, the appropriate message related conditions are recorded in the appropriate controller's BIT word and ISR. Then, Bit 4 of the ISR is set and

an interrupt generated. Now it may be that during bus operation the BIU detects a Loop-Test error, DMA error or Power-On-Reset. In any of these cases no retry is attempted. Here the appropriate condition is recorded in bits 14 thru 16 of the BIT word. Then, bit 4 and bit 14 of the ISR are set and an interrupt generated. There is a second way of programming an interrupt: the OP code of the instruction pair can be set to require the BIU to halt. In this situation , the BIU decodes the requirement and executes it by setting bit 1 of the ISR and then generating the interrupt.

A halt-interrupt condition occurs when the abort control code is sent to Chip #2. In this case, the BIU aborts whatever activity it may be engated in, sets bit 2 of the ISR, and interrupts the host.

Besides the two interrupts available via the stored program instructions and the interrupt via the abort command, a graceful halt interrupt is available to the host via control code 0111. Here the host can request the BIU halt operation. The BIU then finishes its present operation, sets bit 2 in the BIT word, sets bit 3 in the ISR, and interrupts the host. The graceful halt is executed identically to the program controlled interrupt; only the indicator is different.

Bit 5 of the ISR is set and an interrupt generated when the BIU discovers an instruction pair contains the same device address in both instruction words. This check is made during command generation and, when discovered, BIU operations halt without ever beginning data bus transmission.

Bit 6 of the ISR is set and an interrupt generated by the BIU when a mode command requiring mode data has been executed. While attempting to acquire the mode data, the controller may detect a message error or status word exception, ME or Subsystem Busy = 1. Under any of these conditions programmed message retrys are attempted. If the bus operation is ultimately unsuccessful, the appropriate message related conditions are recorded in bits 7 thru 13 of the controller's BIT word. Then, bit 6 of the ISR is set and an interrupt generated. Now it may be that during bus operation the BIU detects a Loop-Test error, DMA error or Power-On-Reset. In any of these cases, no retry is attempted. Here the appropriate condition is recorded in bits 9 through 16 of the BIT word. Then, bit 14 of the ISR is set and an interrupt generated.

Bits 7 and 8 of the ISR are associated with the execution of an asynchronous message. Bit 8 indicates the BIU participated in an asynchronous message; bit 7 = 1 indicates the receiver of the message. The BIU processes these bits whenever it generates a command word with subaddress = 30. After executing the message associated with this command, the BIU generates an interrupt to the host. Treatment accorded message errors, specific status word exceptions, etc. is identical to that used for ISR bit 6 in the paragraph above.

Bit 10 thru 13 of the ISR is set and an interrupt generated when the status word received contains an interrupt condition Treatment accorded message errors, specific status word exceptions, etc. are identical to that used for ISR bit 6 above. The conditions in the returned status word which interrupt the controller include T/F, Service Request, Subsystem Flag, Dynamic Bus Control Accept = 1. It is assumed that automatic message retrys would not be scheduled in sensitive cases, e.g., use of the Dynamic Bus Control mode command.

1.2.1.3.2 Interrupts Generated in the Remote Terminal

In paragraph 1.2.1.3.1 the text describes how message errors detected by the BIU are transferred from BIU #1's error register into BIU #2's BIT register. This same process occurs in the remote terminal. Once a transfer is made, the remote controller tests for the presence of Power-On-Reset, DMA errors, or Loop-Test errors. If any of these are present, BIU will generate an interrupt. These are the only message-error related failures which can cause interrupt generation in the remote terminal.

Besides the above, BIU #2 as part of the remote controller configuration, generates interrupts in response to other conditions described below.

Bit 2 of the ISR is set and an interrupt generated when the abort command (control code 1111) is given to BIU #2. The host can use this command to stop all operation without regard to where the BIU may be in its sequence.

Bit 5 of the ISR is set and an interrupt generated when the RT BIU receives a valid message containing the synchronize mode command (without data word).

Bit 6 of the ISR is set and an interrupt generated when the RT BIU receives any of the mode commands, 10000 thru 11111 provided that the T/R bit of the mode command is a zero. Under such conditions, mode data is waiting for the host in BIU #2's Mode Data Register.

Bits 7 and 8 of the ISR are associated with the execution of an asynchronous message. Bit 8 indicates the BIU participated in an asynchronous message. Bit 7=1 indicates the BIU was the transmitter and bit 7=0 indicates the BIU was the receiver of the message. The BIU processes these bits whenever it receives a command word with subaddress = 30. After successfully executing the message associated with this command, the BIU generates an interrupt to the host.

Bit 9 of the ISR is set and an interrupt generated when the synchronize mode command (with data word) is received. Upon reception of this command, minor cycle time information is waiting for the host in BIU #2's Master Function Register.

1.2.1.3.3 Scenario Used in Interrupt Generation

When an interrupt is generated by the BIU, BIU #2 signals the host via its Interrupt Request line that the BIU needs service. Just before requesting service, BIU #2 sets the Busy/Continue bit in its Processor Control Register (PCR) and in BIU #1's Status Register. After generating the request, BIU #2 monitors the busy bit waiting for a change of condition.

In a remote controller BIU, any command sent to it is implemented by simply returning the status word with the busy bit set; no DMA activity occurs.

In either controller BIU, the activity allowed during the busy condition consists of:

a) monitoring the GO and Busy bits, and
b) implementing the control codes required by the host of BIU #2.

The control codes available to the host are:

0000	Load	Mode Data Register	(MDR)	
0001	Load	Master Function Register (Master)	(MFR)	
0010	Load	Instruction Address Register	(IAR)	
0011	Load	Base Address Register	(BAR)	
0100	Load	Processor Control Register	(PCR)	(both BIUs)
0101	Load	Status Word Data	(SWD)	
0110	Load	Built-In-Test Register	(BIT)	
0111	Halt (graceful)			
1000	Output	MDR		
1001	Output	Recv Status (Mstr)/MFR (RT)		
1010	Output	IAR		
1011	Output	Xmit Status (Mstr)/BAR (RT)		
1100	Output	PCR		
1101	Output	ISR		
1110	Output	BIT		
1111	Abort			

These codes give the host control of the BIU during control-code initiated or power-up or power-dropout initiated busy states.

When BIU #2 initializes itself, it sets bit 14 (the POR bit) in BIT (see Figure 1.2.1.3.1-1). It then clears the ISR and other bits in BIT and sets the Busy and No-Go bits of the PCR to busy (0) and No-Go (0). Finally, it flags its condition by setting its interrupt line active. While in the initialized state, BIU #2's registers may be read or written. The PCR is somewhat special. When loading the PCR, both BIU #1 and BIU #2 accept data from their respective I/O ports. The control code, Load PCR, sent to BIU #2, together with the control code strobe, causes BIU #2 to generate a

FIGURE 1.2.1.3.3-1
PROCESSOR CONTROL WORD FORMAT

code-execute strobe to BIU #1. Then, both BIUs load their respective PCRs. Looking at the format for the PCR given in Figure 1.2.1.3.3-1, bits 8 and 16 are used to alert BIU #1 that the data coincident with the code-execute strobe is PCR data. If the PCR word from the host has Busy and No-Go bits set to busy and no-go, BIU #1 will be set to the busy state and, regardless of its previous state, BIU #1 will now respond to all valid commands with the status word showing the busy status bit set. To properly enter the BIU into an operational scenario, BIU #2's BAR, IAR and MFR should be loaded; then the PCR of both BIU #1 and #2 should be loaded. To remove the BIU from the active state to the busy state, control code 1111 (halt gracefully) should be sent to BIU #2 BIU #2 will complete message processing if a message is present, set the BIU into the busy state, and then interrupt the host At this point any of the registers of interest can be read and reloaded if necessary. Finally, PCRs should be loaded to re-enter active operation.

1.3 Interface

The user interface for the BIU will vary as to the configuration used. In this section enough data will be supplied to allow the interface design necessary to integrate a BIU (or BIU's) into the host electronics. The data will be broken down into I/O electrical characteristics, chip 1 timing, chip 2 timing, and chip-set system characteristics.

1.3.1 Electrical Characteristics

The input/output requirements in Table 1.3.1 are designed to allow a CMOS system, a Low Power Schottky system, or a CMOS/Low Power Schottky system. Serious considerations should be observed as far as I/O loading vs. data rates.

1.3.2 Pin Descriptions

1.3.2.1 BIU #1 Pin Description

See Table 1.3.2.1

1.3.2.2 BIU #2 Pin Description

See Table 1.3.2.2

1.3.3 BIU #1 Timing Characteristics

The timing information presented herein is the required input timing and the supplied output timing of BIU #1 only. This information should be used when BIU #1 is used in the stand-alone configuration or when host supplied interface appears between BIU#1 and BIU #2. The BIU #1 timing is as presented in Figure 1.3.3.

1.3.4 BIU #2 Timing Characteristics

The timing information presented herein is the required input timing and the supplied output timing of BIU #2 only. This information should be used when host supplied interface appears between BIU #1 and BIU #2 or when electronics other than that described in Paragraph 1.3.5 appears between BIU #2 and the host. The BIU timing is as presented in Figure 1.3.4.

The BIU I/Os can be divided into the following types. Pin-out drawings are given in Figure 1.

TYPE 1

The signals listed below are Type 1 I/Os:

Busy/Disable
Code Execute Strobe
Cmd Wd Load (C)/Send Status (R)
Cmd/Status Word Present
Message Complete
Disable Host Interface
Select
Word Count (5 lines)
Load Address Register
Interrupt Request
Control Code In (4 lines)
Control Code Strobe

These signals have the following characteristics:

- An output of one BIU chip must be capable of driving the same-named input of the other BIU chip or a CMOS load and simultaneously driving two LS TTL loads.

  $V_{OL} \leq 0.4V$ @ $I_{OL} = 800\ \mu A$; $V_{OH} \geq V_{CC} - 0.4V$ @ $I_{OH} = 100\ \mu A$

- Capacitive loading of the Type 1 outputs is 50 pf.
- Rise time for Type 1 outputs must be $\leq$ 100 nsec.
- Fall time for Type 1 outputs must be $\leq$ 100 nsec.
- Type 1 inputs must respond to input voltage levels as follows:

	MIN	MAX	
V_{IH}	V_{CC} - 1.25 V	V_{CC}	Logic 1
V_{IL}	0V	0.5V	Logic 0

- Rise and Fall times driving these inputs will be less than 100 nsec.

ELECTRICAL CHARACTERISTICS
TABLE 1.3.1

TYPE 2

The signals listed below are Type 2 I/Os:

	BIU #1	BIU #2
DMA Request	output	in-out
DMA Grant	input	in-out
DMA Read	output	in-out
DMA Write	output	in-out
DMA Acknowledge	input	in-out
Error Present/ME ORD	in-out	in
On Line/Off Line		in-out

These signals have the following characteristics:

- An output of one BIU chip must be capable of driving the same-named input of the other BIU chip or a CMOS load and simultaneously driving two LS TTL loads.

  $V_{OL} \leq 0.4V$ @ $I_{OL} = 800\ \mu A$; $V_{OH} \geq V_{CC} - 0.4V$ @ $I_{OH} = 100\ \mu A$

- Capacitive loading of the Type 2 outputs is 50 pf.
- Rise time for Type 2 outputs must be $\leq$ 100 nsec.
- Fall time for Type 2 outputs must be $\leq$ 100 nsec.
- Type 2 inputs must respond to input voltage levels as follows:

	MIN	MAX	
V_{IH} =	V_{CC} - 1.25 V	V_{CC}	Logic 1
V_{IL} =	0V	0.5V	Logic 0

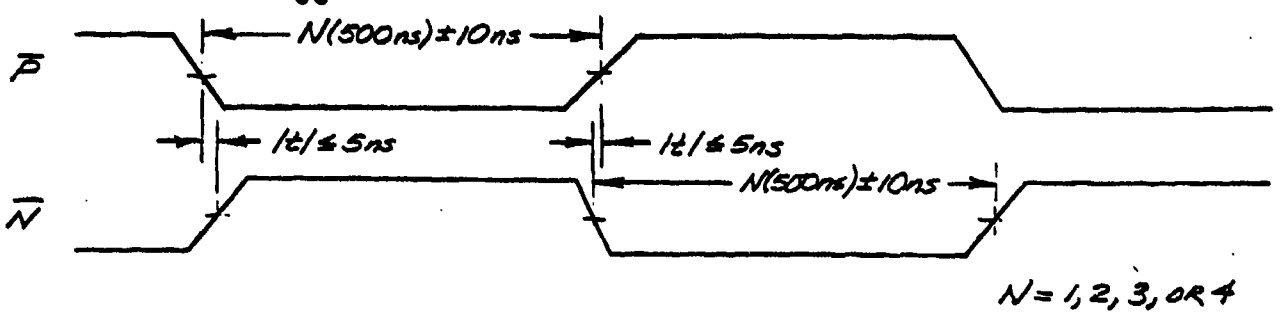
- Rise and Fall times driving these inputs will be less than 100 nsec.

TYPE 3 Baseband rate = 1 MHz

The signals listed below are Type 3 outputs:

Manchester Out (2 lines)

- These signals must drive two LS loads. The $V_{OL} \leq 0.4V$ @ I_{OL} - 800 µA; $V_{OH} \geq V_{CC} - 0.4V$ @ I_{OH} = 100 µA.
- Capacitive load ≤ 25 pf.
- Rise time ≤ 40 ns @ 25 pf load
- Fall time ≤ 40 ns @ 25 pf load
- Symmetry ≤ 5 ns with similar 25 pf loads measured between 50% of V_{CC} points and pulse width of ±10 ns as shown:



The signals listed below are Type 3 inputs:

Manchester IN
Clock 1
Clock 2
Clock (10 MHz max)

- Input V

	MIN	MAX
V_{IL} =	-0.3 volts	0.5 volts
V_{IH} =	V_{CC}-0.5 volts	V_{CC}+0.3 volts

- Supplied rise and fall tr ≤ 25 ns, tf ≤ 25 ns
- Supplied symmetry. For the N(500ns)±150 ns zero crossing signal received by the receiver, a signal of N(500ns)±175 ns pulse width measured from 50% of V_{cc} points shall be supplied to the Manchester In Port. The clocks shall be within a 50% ±15% duty cycle.

ELECTRICAL CHARACTERISTICS
TABLE 1.3.1

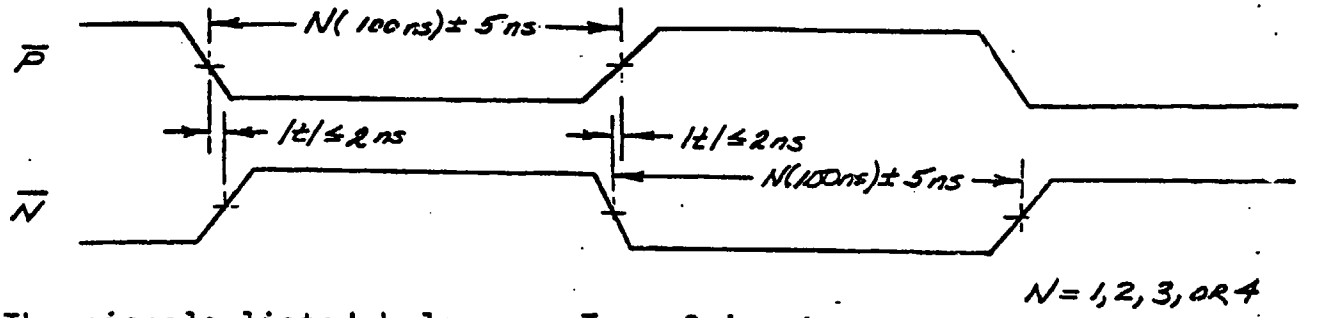
(cont)

TYPE 3 Baseband Rate = 5 MHz

The signals listed below are Type 3 outputs:

Manchester Out (2 lines)

- These signals must drive two LS loads. The $V_{OL} \leq 0.4V$ @ I_{OL} - 800 µA; $V_{OH} \geq V_{CC} - 0.4V$ @ I_{OH} = 100 µA.
- Capacitive load ≤ 25 pf.
- Rise time ≤ 10 ns @ 25 pf load
- Fall time ≤ 10 ns @ 25 pf load
- Symmetry ≤ 2 ns with similar 25 pf loads measured between 50% of V_{CC} points and pulse width of ±5 ns as shown.



The signals listed below are Type 3 inputs:

Manchester IN
Clock 1
Clock 2
Clock (10 MHz max)

- Input V

	MIN	MAX
V_{IL} =	-0.3 volts	0.5 volts
V_{IH} =	V_{CC}-0.5 volts	V_{CC}+0.3 volts

- Supplied rise and fall tr ≤ 25 ns, tf ≤ 25 ns
- Supplied symmetry. For the N(100 ns) ±30 ns zero crossing signal received by the receiver, a signal of N(100 ns) ±35 ns pulse width measured from 50% of V_{CC} points shall be supplied to the Manchester In Port. The clocks shall be within a 50% ±15% duty cycle.

ELECTRICAL CHARACTERISTICS
TABLE 1.3.1

(cont)

TYPE 4

The I/O Bus comprises the Type 4 I/O.

- When a BIU chip drives the I/O Bus it must be capable of driving two LS TT L loads and simultaneously driving the same named port of the other BIU chip type.

  $V_{OL} \leq 0.4V$ @ $I_{OL} = 800\ \mu A$; $V_{OH} \geq V_{CC} - 0.4V$ @ $I_{OH} = 100\ \mu A$

- A BIU chip using the I/O bus as an input must respond to voltage levels as follows:

	MIN	MAX	
V_{IH} =	$V_{CC} - 1.25$	V_{CC}	Logic 1
V_{IL} =	0V	0.5V	Logic 0

- Capacitive loading of Type 4 outputs is 75 pf.

- Rise time for Type 4 outputs must be $\leq$ 150 nsec.

- Fall time for Type 4 outputs must be $\leq$ 150 nsec.

- Under the above loading conditions, the I/O ports of BIU Chip #1 must have built-in pull-up capability. When the I/O Bus is not being driven by BIU #1 of BIU #2 tri-state drivers or by any other source, BIU #1 pull-ups must pull the bus from the zero logic level to the one logic level within 1 µsec.

ELECTRICAL CHARACTERISTICS
TABLE 1.3.1

(cont)

TABLE 1.3.2.1-BIU PIN FUNCTION DESCRIPTION

PIN	FUNCTION
1	V_{CC} - Supply pin - +5V $\pm$ 5%.
2	I/O 2^8 - Bidirectional data bus utilized for command and data transfer between the host electronics including HS-3274 or equivalent and HS-3273.
3	I/O 2^9 - Bidirectional data bus utilized for command and data transfer between the host electronics including HS-3274 or equivalent and HS-3273.
4	I/O 2^{10}- Bidirectional data bus utilized for command and data transfer between the host electronics including HS-3274 or equivalent and HS-3273.
5	I/O 2^{11}- Bidirectional data bus utilized for command and data transfer between the host electronics including HS-3274 or equivalent and HS-3273.
6	I/O 2^{12}- Bidirectional data bus utilized for command and data transfer between the host electronics including HS-3274 or equivalnet and HS-3273.
7	I/O 2^{13}- Bidirectional data bus utilized for command and data transfer between the host electronics including HS-3274 or equivalent and HS-3273.
8	I/O 2^{14}- Bidirectional data bus utilized for command and data transfer between the host electronics including HS-3274 or equivalent and HS-3273.
9	I/O 2^{15}- Bidirectional data bus utilized for command and data transfer between the host electronics including HS-3274 or equivalent and HS-3273.
10	$\overline{\text{DMA ACKNOWLEDGE}}$ - Input from host electronics indicating that a DMA write cycle has been completed or, during a read cycle, that data for the BIU is present on the I/O bus.
11	$\overline{\text{DMA WRITE}}$ - Output to host electronics issued following receipt of $\overline{\text{DMA GRANT}}$ indicating that the I/O bus contains data to be written to memory.
12	$\overline{\text{DMA GRANT}}$ - Input from host electronics following issuance of $\overline{\text{DMA REQUEST}}$ indicating that the I/O bus is inactive and that the host is ready to proceed with the DMA.
13	$\overline{\text{DMA READ}}$ - Output to host electronics issued following receipt of $\overline{\text{DMA GRANT}}$ indicating that the HS-3273 desires data from its host's memory.
14	$\overline{\text{DMA REQUEST}}$ - Output to host electronics indicating that HS-3273 is ready to perform a DMA transfer.
15	$\overline{\text{BUSY/DISABLE}}$ - Input which indicates to the BIU that the host is busy. This signal inhibits DMA activity within HS-3273; it will also result in setting the busy bit in the status word and only returning the status word if the $\overline{\text{BUSY/DISABLE}}$ line is active during the trailing edge time of $\overline{\text{CMD WD LD(C)/SEND STATUS WD(RT)}}$.

TABLE 1.3.2.1-BIU PIN FUNCTION DESCRIPTION

16 $\overline{\text{WORD COUNT } 2^0}$ - Output and least significant bit of a word indicating the number of DMA cycles required to fulfill a command.

17 $\overline{\text{WORD COUNT } 2^1}$ - Output and 2^1 bit of a word indicating the number of DMA cycles required to fulfill a command.

18 $\overline{\text{WORD COUNT } 2^2}$ - Output and 2^2 bit of a word indicating the number of DMA cycles required to fulfill a command.

19 $\overline{\text{WORD COUNT } 2^3}$ - Output and 2^3 bit of a word indicating the number of DMA cycles required to fulfill a command.

20 $\overline{\text{WORD COUNT2}^4}$ - Output and most significant bit of a word indicating the number of DMA cycles required to fulfill a command.

21 V_{SS} - Circuit ground.

22 $\overline{\text{MESSAGE COMPLETE}}$ - Output to host electronics indicating completion of transmission onto the serial bus or completion of message reception. Once a message handling process is started, HS-3273 implements the appropriate algorithm and always follows that with a message-complete indication.

23 $\overline{\text{CMD WD LD(C)/SEND STATUS WD(RT)}}$ - Input (in Controller Mode) used to stimulate HS-3273 to accept for transmission a command word present on the 16 bit I/O bus. In the Remote Mode, pin 23 is an output used by HS-3273 to indicate a command word for the terminal being processed; in the Remote Mode, HS-3273 expects to receive status-word-related data (Terminal-Fail flag, subsystem flag and service request) on 16-bit I/O bus bits 2^0, 2^1, 2^2, respectively.

24 $\overline{\text{CMD WD/STATUS WD PRESENT}}$ - Output to host electronics indicating that HS-3273 has presented a command or status word on the I/O bus resulting from reception of the beginning of a message.

25 MANCHESTER OUT "T" - True encoder output to serial bus transmitter. Held at logic "1" when HS-3273 encoder is inactive.

26 MANCHESTER OUT "F" - False encoder output to serial bus transmitter. Held at logic "1" when HS-3273 encoder is inactive.

27 $\overline{\text{ERROR PRESENT}}$ - Discrete output to host electronics indicating that an error has been detected in a received or transmitted message. During the time when HS-3273 output is active, $\overline{\text{ERROR PRESENT}}$ becomes an input; a "1" or "0" present on pin 27 during the time of the trailing edge of $\overline{\text{CMD WD/STATUS WD PRESENT}}$ will be transferred into the status word's message-error bit position. This feature allows the RT to indicate to the controller that some aspect of the command word just received was invalid.

TABLE 1.3.2.1-BIU PIN FUNCTION DESCRIPTION

28 $\overline{\text{CODE EXECUTE}}$ - Input from host electronics which enables the HS-3273 command decoder to accept configuration and/or command data present on the I/O bus. The $\overline{\text{CODE EXECUTE}}$ strobe keys on the state of 2^0 of the I/O bus. When $2^0 = 1$ during the strobe time, the data on the I/O bus is considered to be configuration information (see configuration data format); otherwise, HS-3273 interprets I/O bus bits 2^2 and 2^1 as follows:

2^2	2^1	Function
0	0	HS-3273 reset
0	1	Next message will be RT-to-RT (controller only)
1	0	Output Error Data
1	1	(Not Used)

Note, when the command to "output error data" is issued, HS-3273 will respond with data on its lower byte. The data output will remain stable until the host issues a second $\overline{\text{CODE EXECUTE}}$ strobe. This second strobe (with the host's I/O bus drivers in the high impedance state) will unlatch a flip flop in HS-3273 and cause the HS-3273 lower byte I/O bus drivers to enter the high impedance state.

29 $\overline{\text{RESET}}$ - Initializes the HS-3273. HS-3273 is inhibited after receipt of a $\overline{\text{RESET}}$ strobe until HS-3273 is configured by $\overline{\text{CODE EXECUTE}}$ together with appropriate configuration data on the I/O Bus.

30 CLOCK 2 - For data rates greater than 2 Mbps, CLOCK 2 is to be an asynchronous clock at 2X data rate. For data rates less than 2 Mbps, CLOCK 2 is to be grounded.

31 CLOCK 1 - For data rates greater than 2 Mbps, CLOCK 1 is to be a synchronized 2X clock to MANCHESTER IN. For data rates less than 2 Mbps, CLOCK 1 is to be an asynchronous 10X data rate clock.

32 MANCHESTER IN - Input from serial bus received in single-ended bi-phase manchester form.

33 I/O 2^0 - Bidirectional data bus utilized for command and data transfer between the host electronics including HS-3274 or equivalent and HS-3273.

34 I/O 2^1 - Bidirectional data bus utilized for command and data transfer between the host electronics including HS-3274 or equivalent and HS-3273.

35 I/O 2^2 - Bidirectional data bus utilized for command and data transfer between the host electronics including HS-3274 or equivalent and HS-3273.

36 I/O 2^3 - Bidirectional data bus utilized for command and data transfer between the host electronics including HS-3274 or equivalent and HS-3273.

TABLE 1.3.2.1-BIU PIN FUNCTION DESCRIPTION

37 I/O 2^4 - Bidirectional data bus utilized for command and data transfer between the host electronics including HS-3274 or equivalent and HS-3273.

38 I/O 2^5 - Bidirectional data bus utilized for command and data transfer between the host electronics including HS-3274 or equivalent and HS-3273.

39 I/O 2^6 - Bidirectional data bus utilized for command and data transfer between the host electronics including HS-3274 or equivalent and HS-3273.

40 I/O 2^7 - Bidirectional data bus utilized for command and data transfer between the host electronics including HS-3274 or equivalent and HS-3273.

TABLE 1.3.2.1-BIU PIN FUNCTION DESCRIPTION

BIU #1 (HS-3273) PIN LIST

PIN	DESCRIPTION	PIN	DESCRIPTION
1	V_{CC}	21	V_{SS}
2	I/O 2^8	22	$\overline{\text{MESSAGE COMPLETE}}$
3	I/O 2^9	23	$\overline{\text{CMD WD LD(C)/SEND STATUS WD(RT)}}$
4	I/O 2^{10}	24	$\overline{\text{CMD WD/STATUS WD PRESENT}}$
5	I/O 2^{11}	25	MANCHESTER OUT F
6	I/O 2^{12}	26	MANCHESTER OUT T
7	I/O 2^{13}	27	$\overline{\text{ERROR PRESENT}}$
8	I/O 2^{14}	28	$\overline{\text{CODE EXECUTE}}$
9	I/O 2^{15}	29	$\overline{\text{RESET}}$
10	$\overline{\text{DMA ACKNOWLEDGE}}$	30	CLOCK 2
11	$\overline{\text{DMA WRITE}}$	31	CLOCK 1
12	$\overline{\text{DMA GRANT}}$	32	MANCHESTER IN
13	$\overline{\text{DMA READ}}$	33	I/O 2^0
14	$\overline{\text{DMA REQUEST}}$	34	I/O 2^1
15	$\overline{\text{BUSY/DISABLE}}$	35	I/O 2^2
16	$\overline{\text{WORD COUNT } 2^0}$	36	I/O 2^3
17	$\overline{\text{WORD COUNT } 2^1}$	37	I/O 2^4
18	$\overline{\text{WORD COUNT } 2^2}$	38	I/O 2^5
19	$\overline{\text{WORD COUNT } 2^3}$	39	I/O 2^6
20	$\overline{\text{WORD COUNT } 2^4}$	40	I/O 2^7

TABLE 1.3.2.2

BIU #2 PIN DESCRIPTION

SIGNAL NAME	INPUT/OUTPUT	SIGNAL FUNCTION
I/O Bus	Input/Output Tristate	Parallel data path between BIU #2 and any logic to which it is interfaced including BIU Chip #1. Shared with BIU #1.
DMA Request DMA Grant DMA Write DMA Read DMA Acknowledge	Input/Output Tristate (Low Active)	Initiates EMA cycle for instruction words, pointer word, and tag word. Answers BIU #1 DMA cycle for mode code data transfers. DMA Read or DMA Write active during control code operations. No DMA Request or DMA Grant issued. Shared with BIU #1.
Control Code Strobe Control Code Inputs	Inputs (Strobe Low Active)	Codes 0000 → 0110 activate DMA Read output and BIU #2 accepts 16-bit word from host. Codes 1000 → 1110 activate DMA Write output and BIU #2 outputs 16-bit word to host. Code 0111 causes BIU to halt and go busy after message complete. Code 1111 causes BIU to abort and go busy at the time the code is issued.
Interrupt Request	Output (Low Active)	Low active level indicates interrupt. Clear interrupt by loading processor control word to run condition.

TABLE 1.3.2.2 (continued)

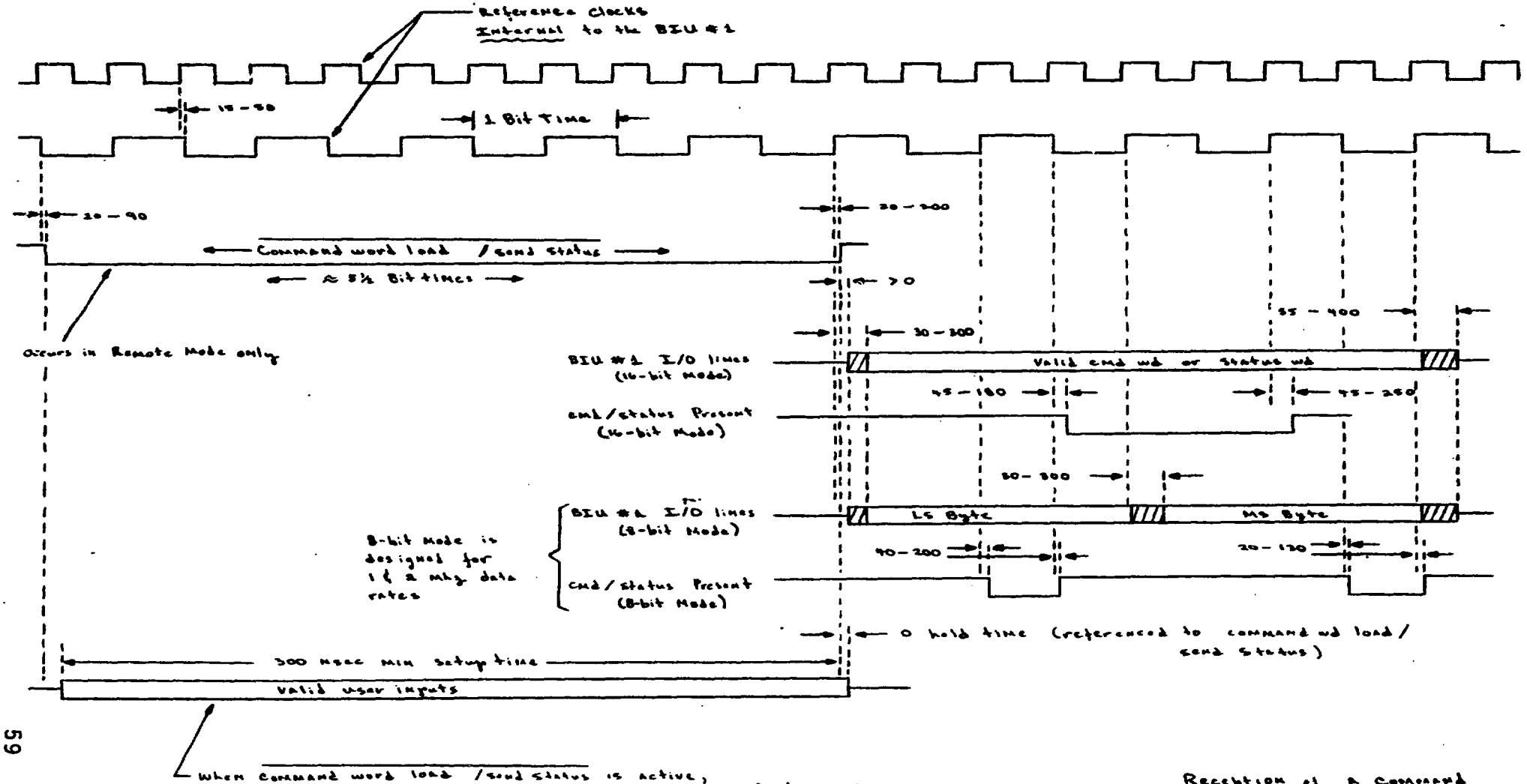
SIGNAL NAME	INPUT/OUTPUT	SIGNAL FUNCTION
Busy/Disable	Output (Low Active)	Disables (tristates) I/O bus and DMA lines in BIU #1. Suppresses command/status present. Sets busy bit in BIU #1 status word if command is received while active. Active due to BIU #2 DMA activity, control abort, or interrupt.
Code Execute Strobe	Output (Low Active)	Code strobe and code (LSB 3 bits of I/O Bus) perform control functions in BIU #1. Functions are RT-RT transfer, error register output, abort, processor control word load.
Message Complete	Input (Low Active)	Signifies to BIU #2 that BIU #1 has completed the on-going message transfer. (Normal or abnormal transfer). Indicates that error present information is available.
Command/Status Present	Input (Low Active)	Signifies that received status word is present on I/O bus (master). Signifies that received command word is present on I/O bus (remote). Signifies time to input MEORD data (remote).

TABLE 1.3.2.2 (continued)

SIGNAL NAME	INPUT/OUTPUT	SIGNAL FUNCTION
Host Interface Disable	Output (Low Active)	Active for DMA of mode code data. Active during control code abort command.
On Line/Off Line	Input/Output (Low Active)	Pulse from "on line" BIU #2 after BIU has entered the run mode. Synchronizes "off line" BIU #2 in redundant operation. At "power on" or after "abort", "on line" BIU is one that has bit 9 of processor control word = "0".
Load Address Register	Output (Low Active)	Active for IW1 address load (master mode). Active for IW2 address load (master mode). Active for pointer address load. Active for data buffer address load. Active for tag word address load.
Error Present/MEORD	Input (Low Active)	Indicates error present from BIU #1. See timing. Low during command/status present time loads illegal command bit in built-in-test register.
Select	Output	Reflects state of bit 6 of IW2. Valid with 750 ns after IW2 DMA is complete.

TABLE 1.3.2.2 (continued)

SIGNAL NAME	INPUT/OUTPUT	SIGNAL FUNCTION
Command Word Load/ Send Status	Input/Output	Output to BIU #1 signifying that a command word to be transmitted is present on I/O bus (master only). Input from BIU #1 requesting service request, subsystem flag and terminal fail status word bits. (remote only).
Clock	Input	Input clock 10 MHz maximum.

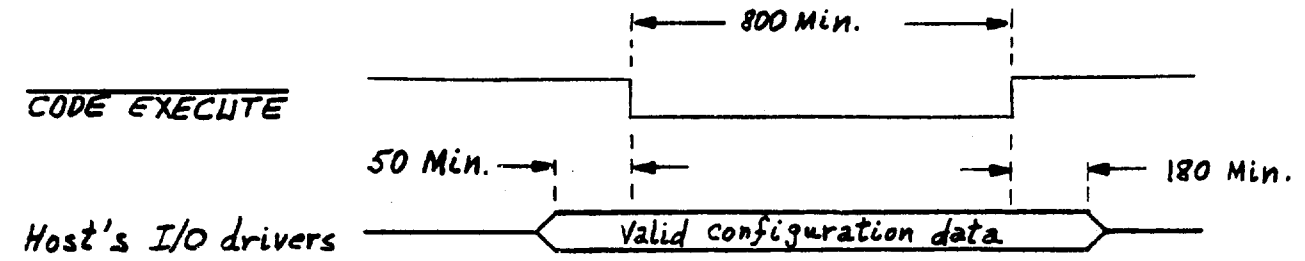


When Command word load / send status is active, the user Must supply inputs on BIU I/O lines, 2^4, 2^1 and 2^0

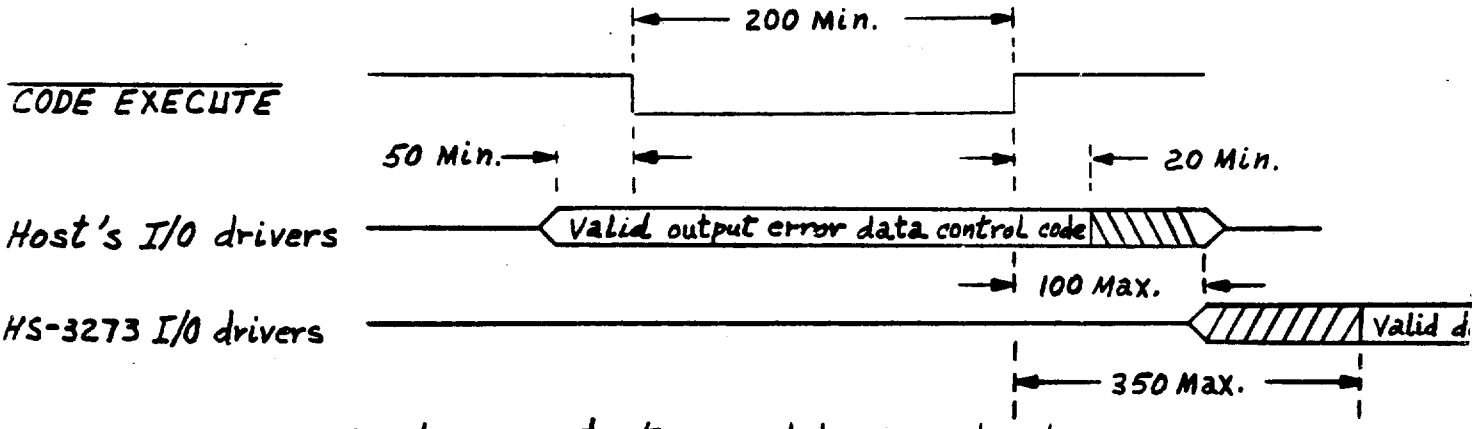
These inputs are positive true and

2^0 represents the Terminal-Fail Flag of the returned status word;
2^1 represents the Subsystem Flag and
2^2 represents the Service Request

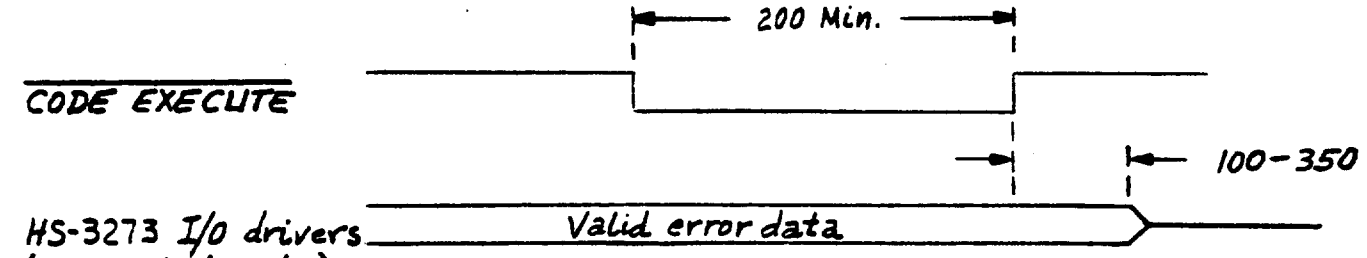
Reception of a Command Word (RT) or status word (C)



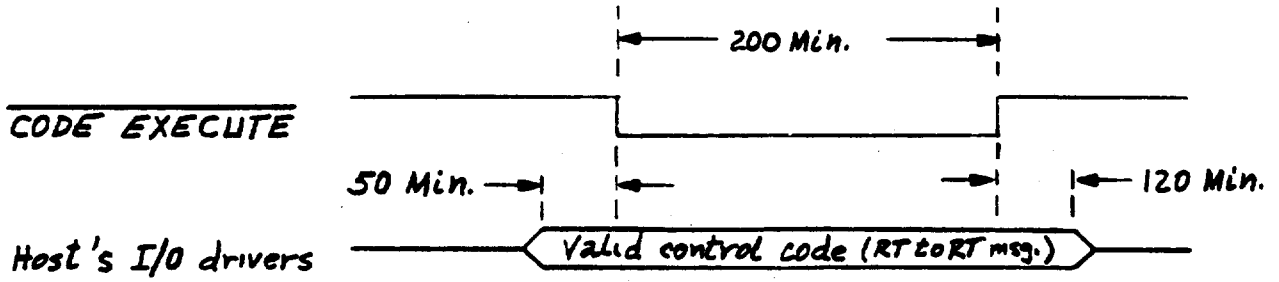
Loading configuration data into HS-3273.



Loading an output error data request into HS-3273

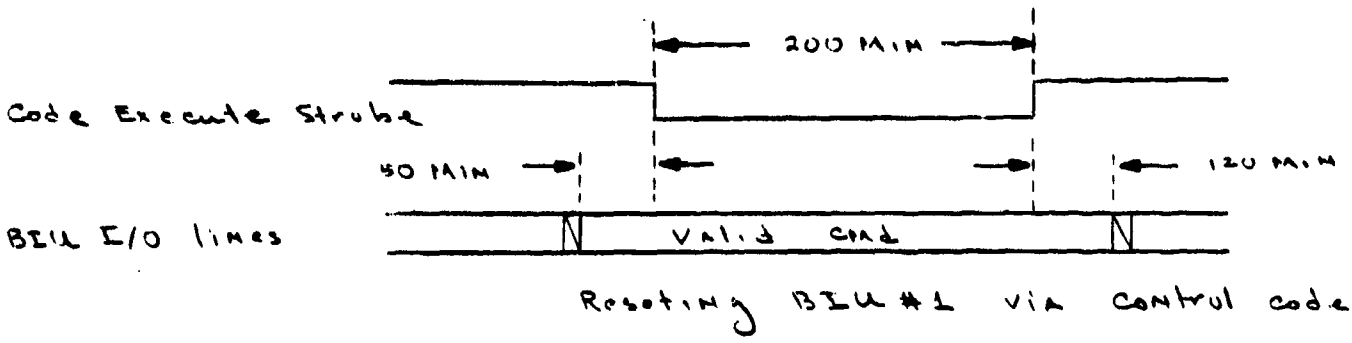


Causing the HS-3273 lower byte to enter Hi-Z state after host has read the HS-3273 error data.



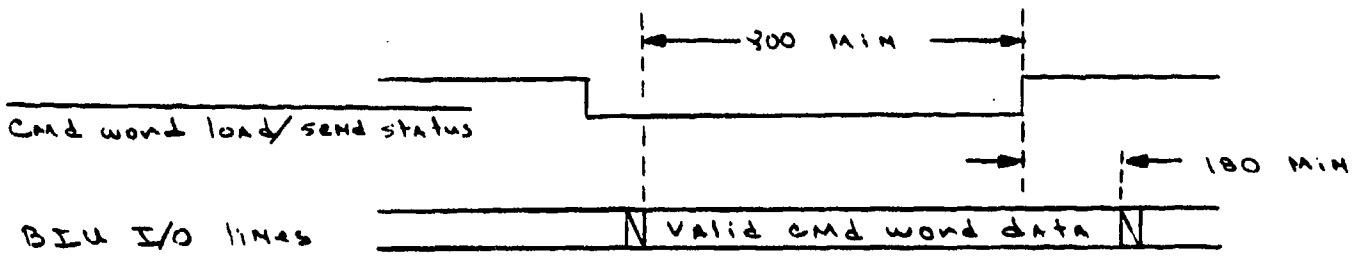
Loading a "next message will be RT-to-RT" request into HS-3273.

Note: All times in nanoseconds.



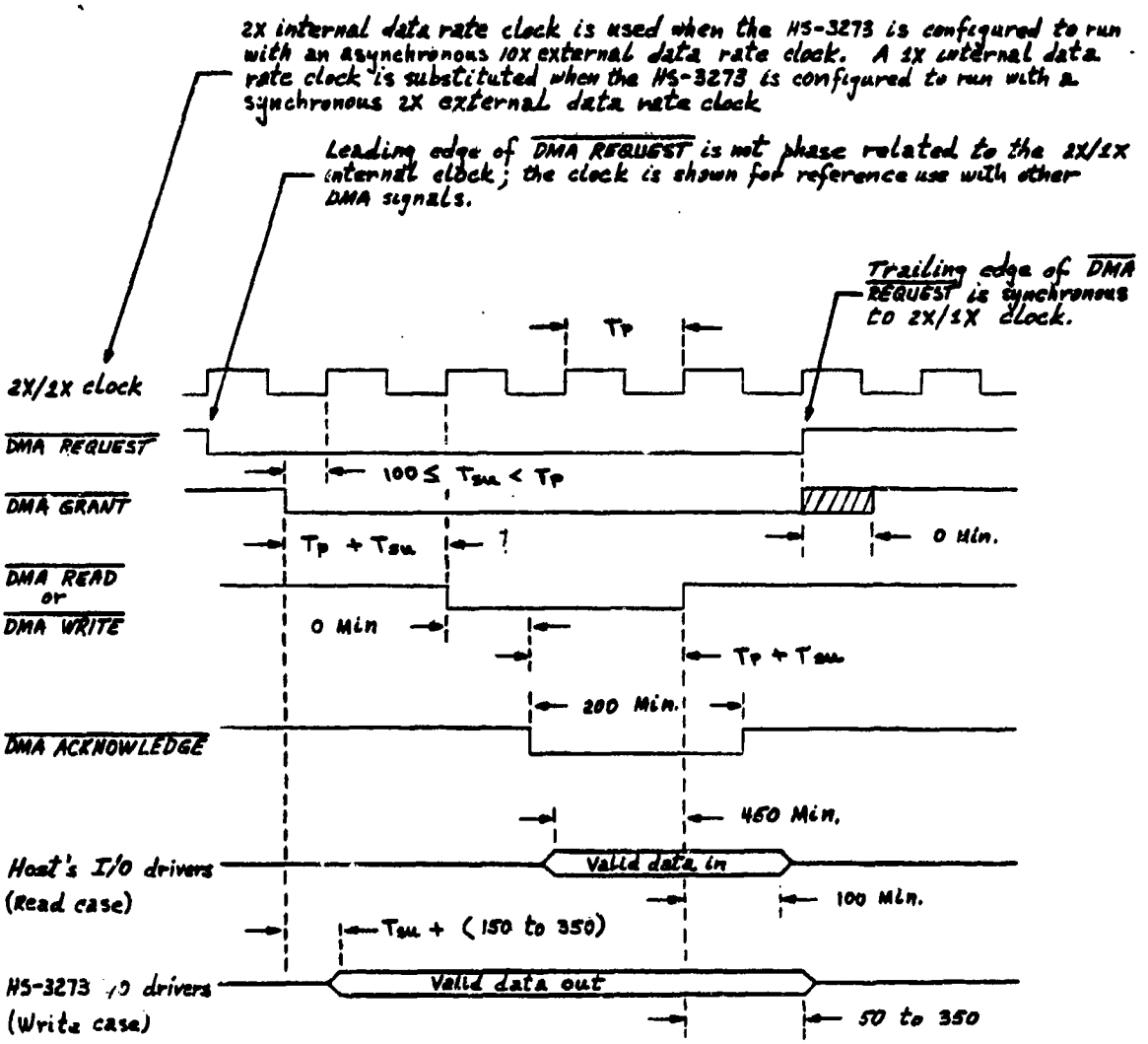
Resetting BIU #1 via control code

Reset BIU #1 via Reset Pin



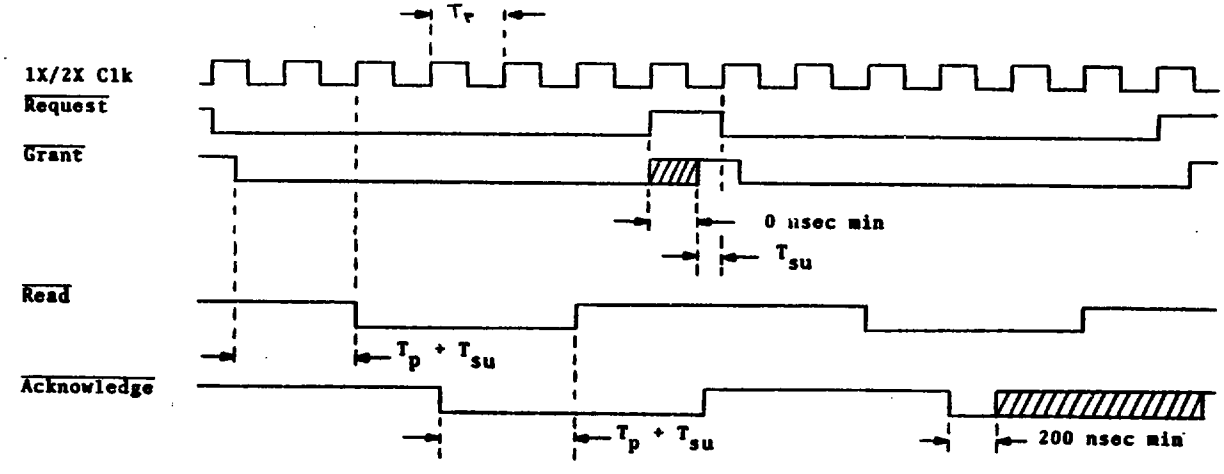
Loading BIU #1 (as controller)
with a command word for transmission

Note: All times in N sec

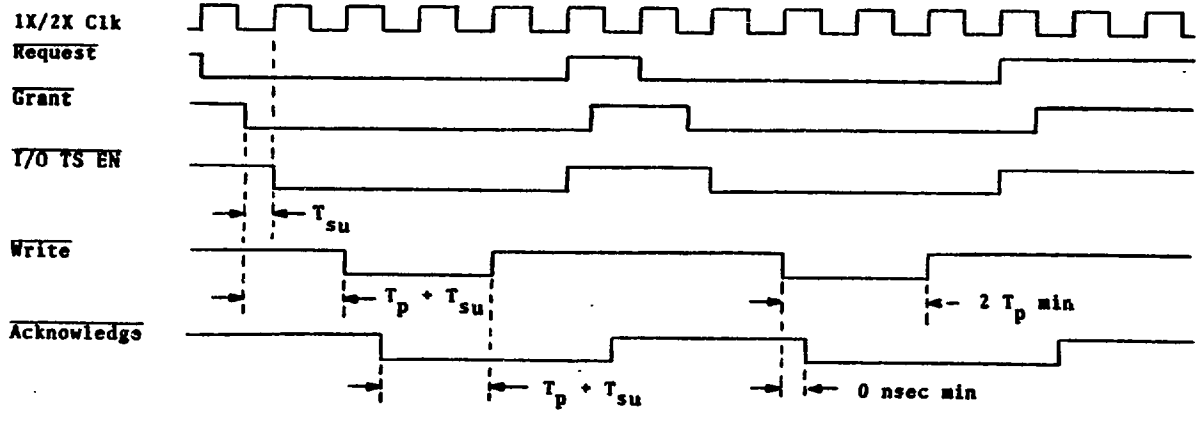


Note: All times in nsec.

DMA SEQUENCE FOR HS-3273
(Configured for 16 bit I/O data bus)

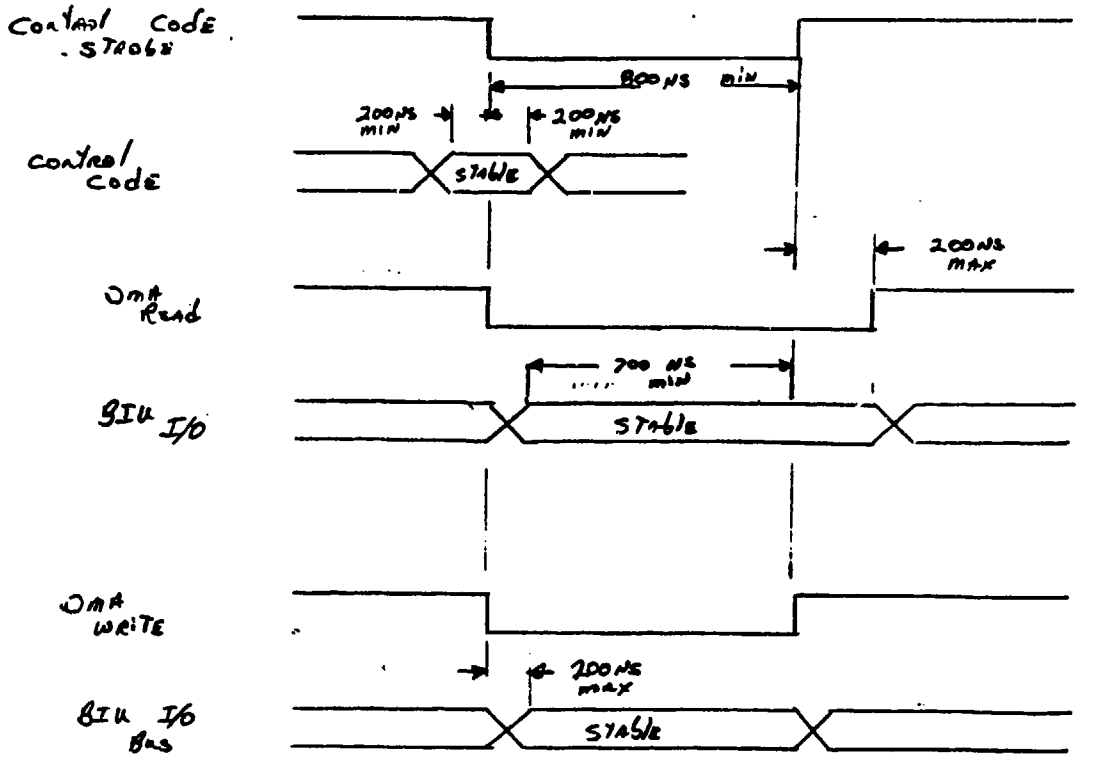


8-BIT MODE (2 READ CYCLES)



8-BIT MODE (2 WRITE CYCLES)

DMA Control Sequence for BIU #1 (NS 32203)



800 NS min
No MAX Limit

Input To BIU
Control codes
0000 → 0111

output from BI
control codes
1000 → 1111

Note: DMA
REQUEST REMAINS
INACTIVE FOR
BOTH CASES ABO

Control Code Timing

BIU #2 DMA Cycle - Normal Cycle
(BIU #2 Initiated)

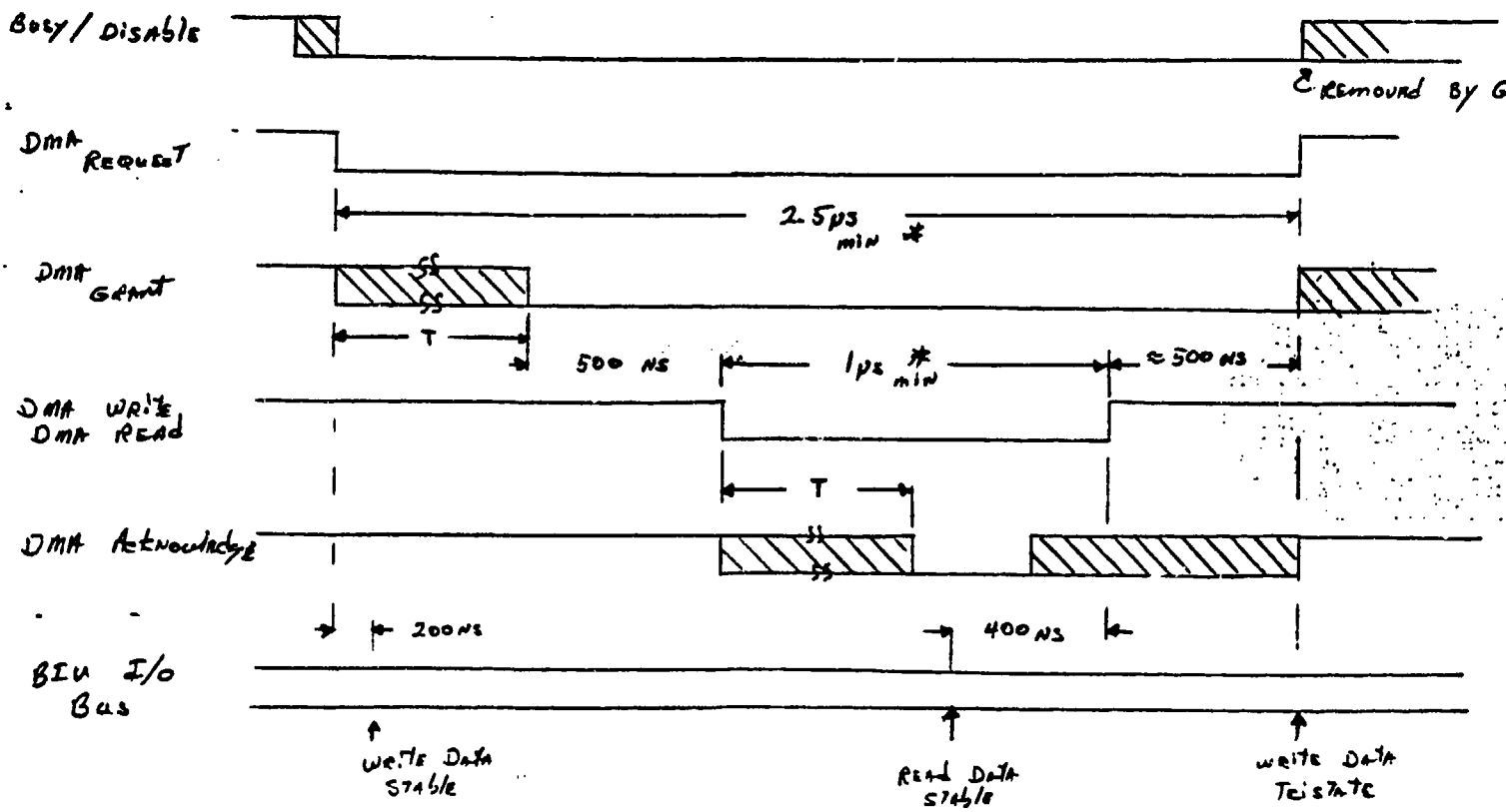
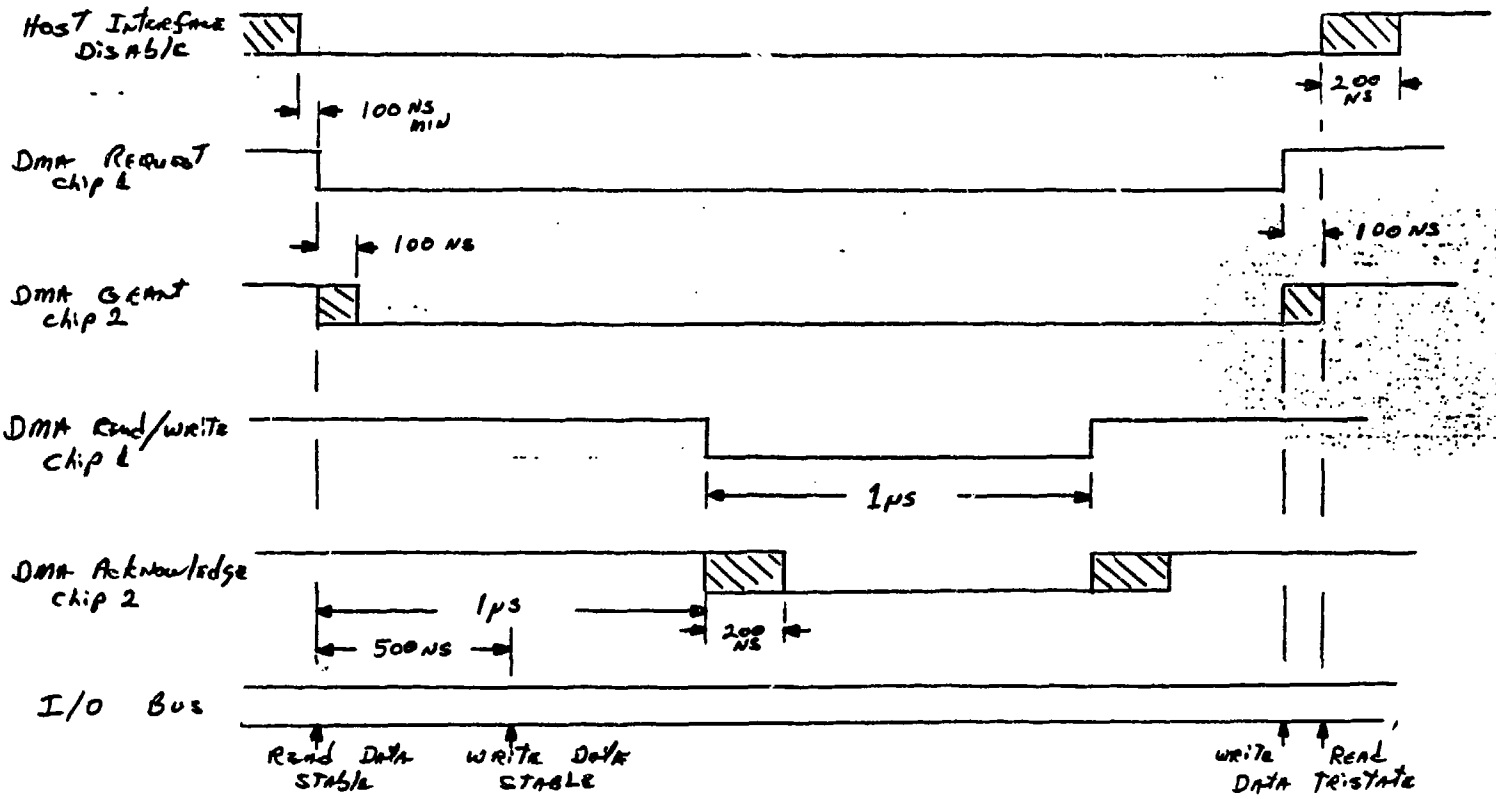
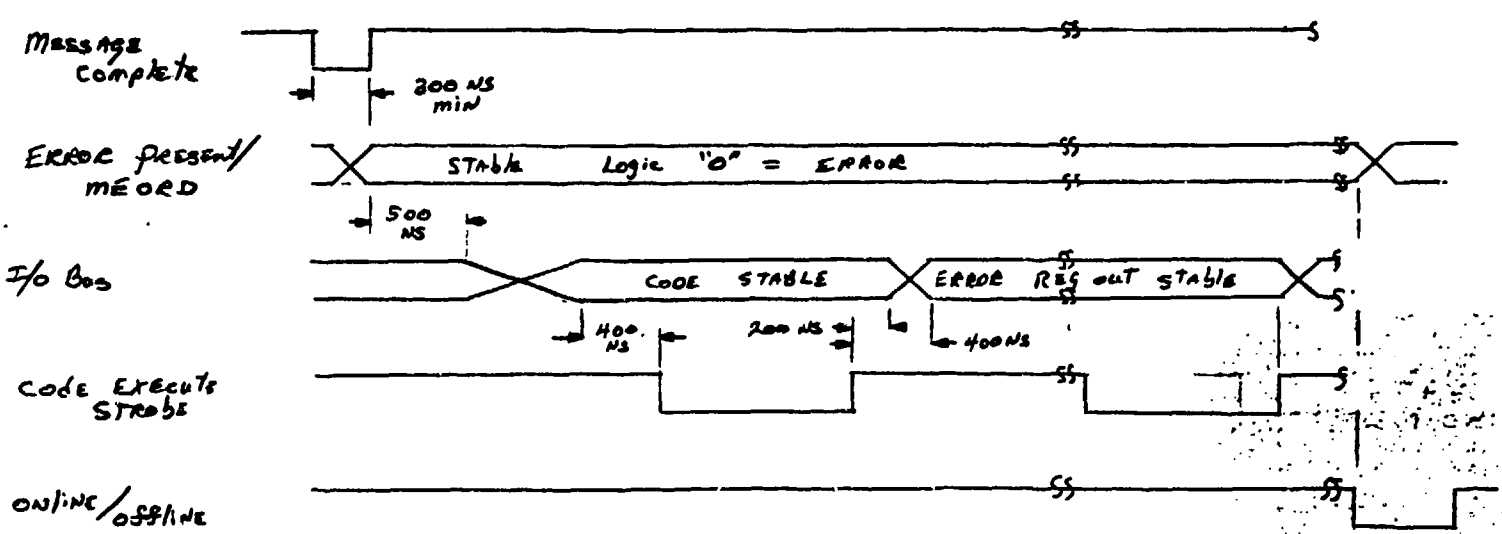


Figure 1.3.4 BIU # 2 Timing



DMA Cycle - Mode Code - Chip 1 Initiated

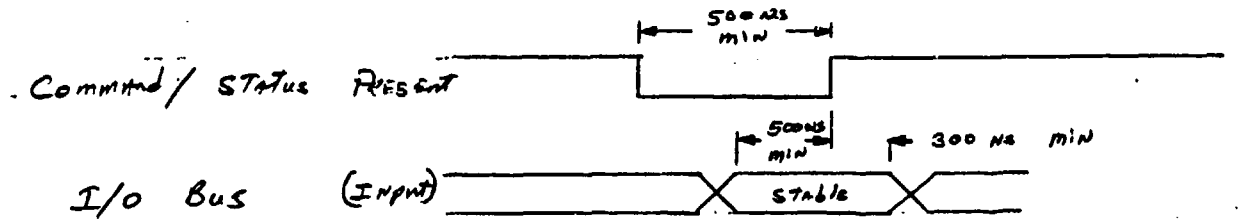
ERROR Read cycle - Chip 2 Read of Chip 1

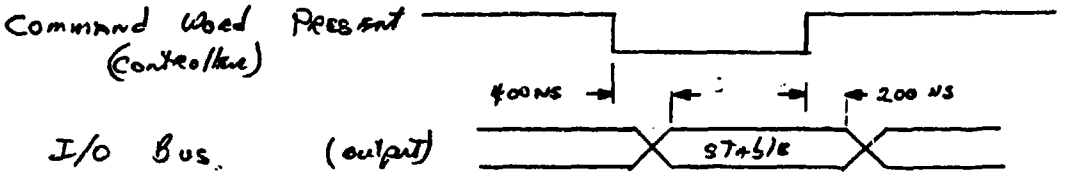


Above for master mode, Remote mode ERROR present need be STABLE only until leading edge of First Code Execute Strobe.

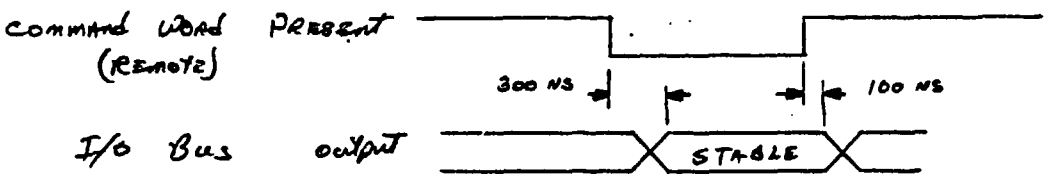
Figure 1.3.4 (cont)

BIU # 2 Timing

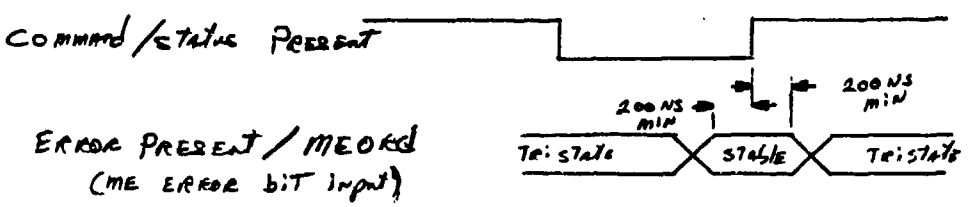




$t_{PW} \approx 900$ NS

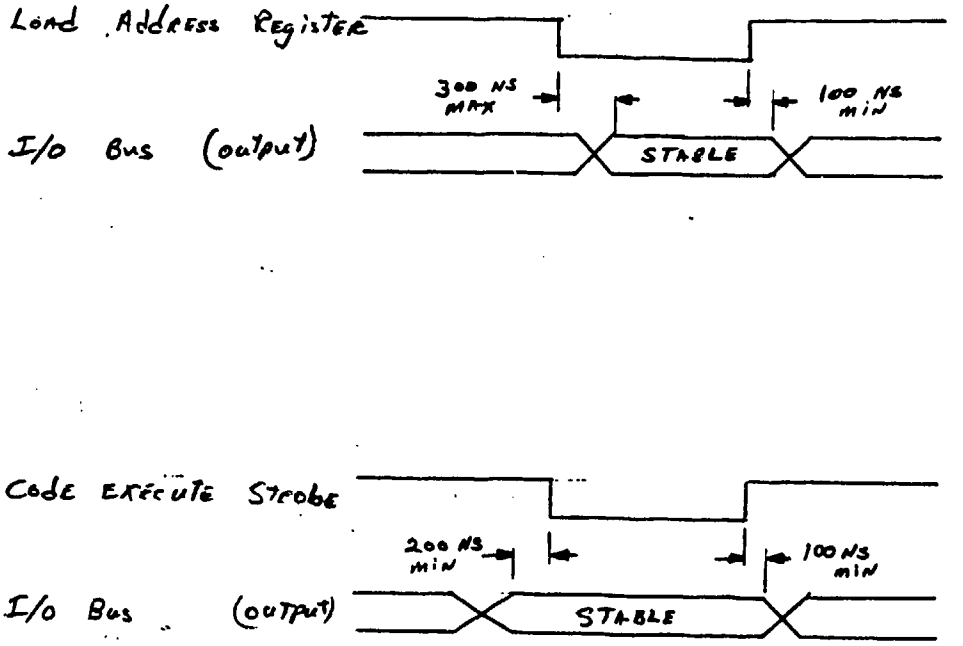


$t_{PW} = 5\ \mu s$ AT 1 MHz



MEORD Driver must Tristate be open Coll

FIGURE 1.3.4 (cont)



$t_{pw} \approx 900$ NS AT 1 MHZ

$t_{pw} = 200$ NS MIN

Figure 1.3.4 (cont)

BIU #2 Timing

1.3.5 BIU Chip-Set "Module" Characteristics

When the BIU chip set is used in a system, certain system design precautions must be made. These primarily involve data transfer characteristics of the BIU's. As described in paragraphs 1.3.2, 1.3.3, and 1.3.4, the BIU not only performs DMA and Discrete Data Transfers to the host, but also between BIU #1 and BIU #2. These transfers must either be expected by the host or be isolated from the host. The following sub-paragraphs describe a BIU chip set with the necessary "isolation interface" to be a stand-alone module.

1.3.5.1 Logic Considerations

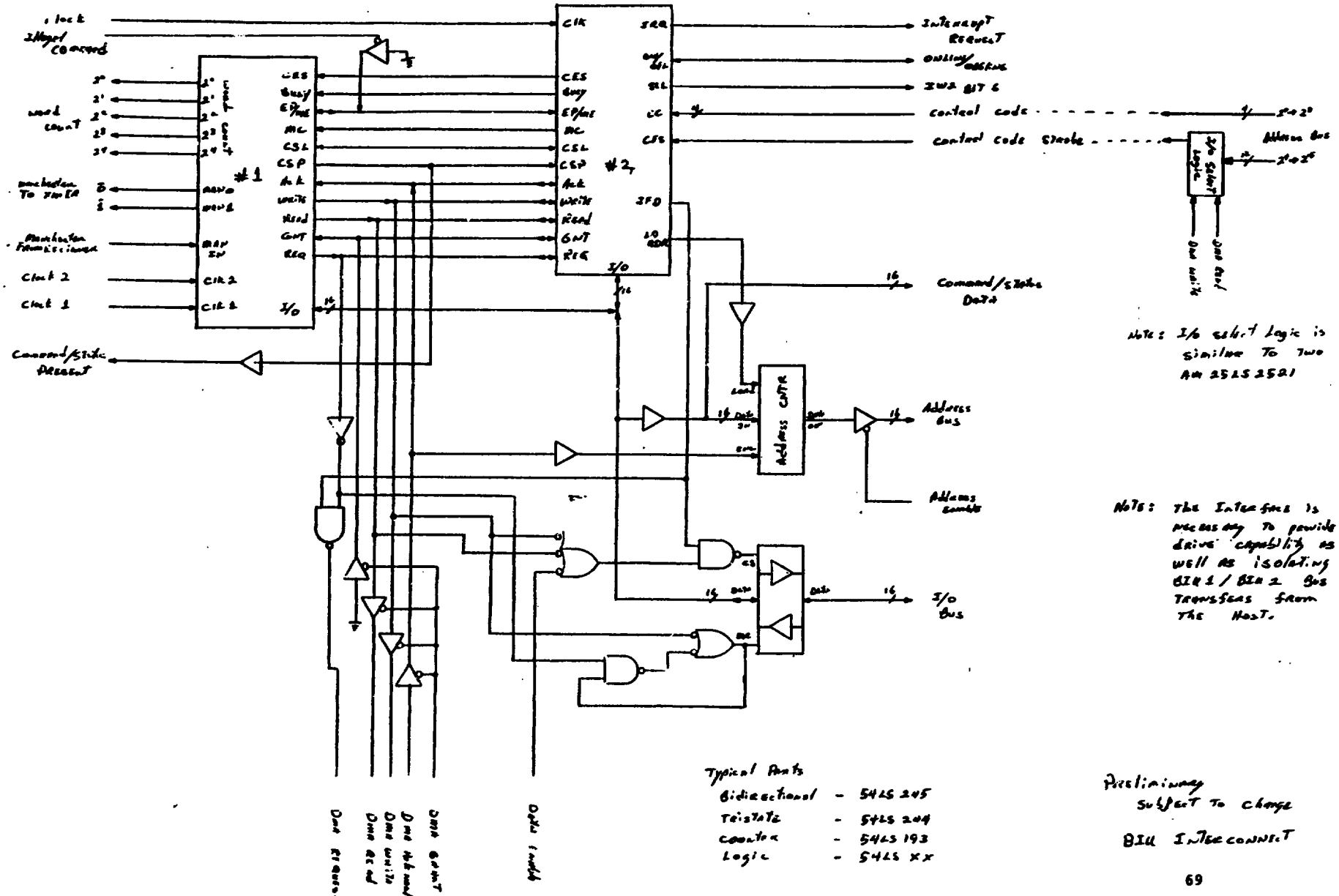
The logic diagram shown in Figure 1.3.5.1 is the recommended minimum interface logic to obtain an "isolated" stand-alone module. All transfers to and from the host would be DMA or Programmed I/O. Provision is also made to allow decode of command/ status words. Logic elements could be CMOS, Low Power Schottky, or any MOS compatible devices.

1.3.5.2 Pin Descriptions

The pin descriptions in Table 1.3.5.2 describe the BIU module to host interconnection only (I/O Bus, Address Bus, DMA and control signals).

1.3.5.3 Timing Characteristics

Again here only the host related signals as in Paragraph 1.3.5.2 will be discussed. This basic timing should give good insight to system design requirements. The timing is as shown in Figure 1.3.5.3.



Note: I/O select logic is similar to two AM 2515 2521

Note: The Interface is necessary to provide drive capability as well as isolating BIU 1 / BIU 2 Bus Transfers from the Host.

Typical Parts

Bidirectional	-	54LS 245
Tri-State	-	54LS 244
Counter	-	54LS 193
Logic	-	54LS xx

Preliminary
Subject To Change

BIU Interconnect

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Figure 1.3.5.1

FIGURE 1.3.5.2

MODULE PIN DESCRIPTION

SIGNAL NAME	INPUT/OUTPUT	SIGNAL FUNCTION
Command/Status Data	Output	• Buffered internal data bus • Used to external decode mode codes or illegal command • Used with command/status present • See BIU #1 timing
Address Bus	Output (Tri-State)	• Output of DMA address counter • Data enabled by address enable
Address Enable	Input (Low Active)	• Enables 16-bit address counter output • Normally connected to DMA grant
I/O Bus	I/O (Positive Logic)	• 16-bit data path between BIU and host • See timing
Data Enable	Input (Active Low)	• Enables bi-directional interface for DMA operation • Normally connected to DMA grant
DMA Request DMA Grant DMA Read DMA Write DMA Acknowledge	Output Input Output Output Input (Active Low)	• DMA cycle for all instruction words, pointer words, tag words and bus data • DMA originate from BIU #1 or BIU #2

FIGURE 1.3.5.2

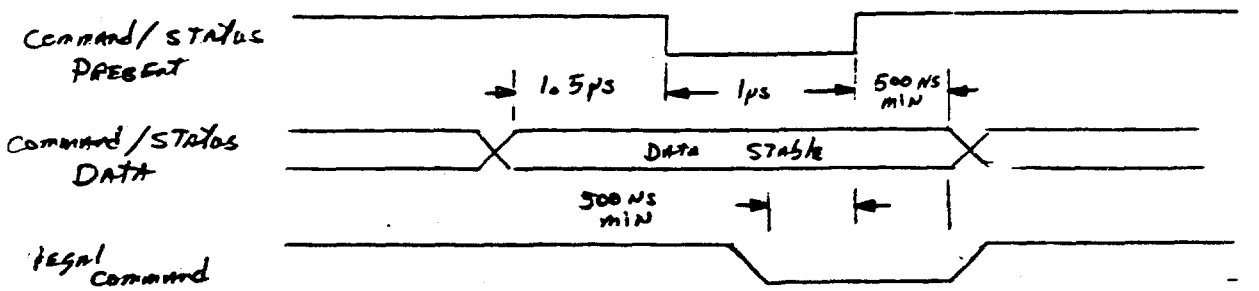
MODULE PIN DESCRIPTION

SIGNAL NAME	INPUT/OUTPUT	SIGNAL FUNCTION
Clock	Input	• Master Clock for BIU #2 • Frequency 10 MHz (max)
Illegal Command	Input (Low Active)	• Active when remote command received is not executable
Word Count Out	Output (Positive Logic)	• Counts from zero to the # of words received or transmitted • Used to steer hardware registers in a "dumb" remote typically
Manchester to XMTR	Output (Active Low)	• See BIU #1 timing • Drive to 1553B Transmitter
Manchester from RCVR	Input (Positive Logic)	• See BIU #1 timing • Unipolar input from 1553B receiver
Clock 1	Input	• Ten times data rate when internal sampling used • Two times data rate when external sampling used • Synchronous with data in external sample mode • See BIU #1 timing
Clock 2	Input	• Two times data rate when in external sample mode • Asychronous • Not used in internal sample mode

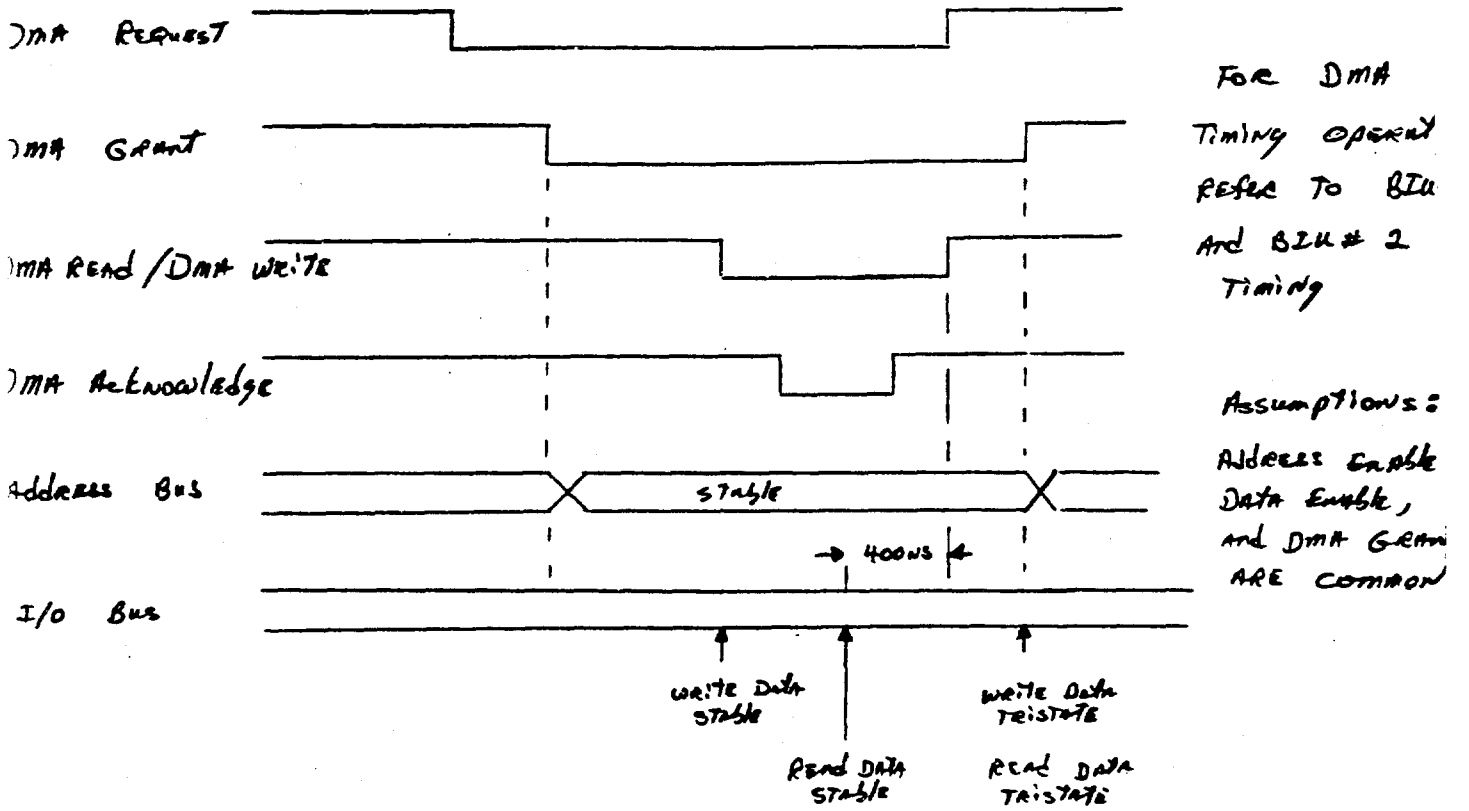
FIGURE 1.3.5.2

MODULE PIN DESCRIPTION

SIGNAL NAME	INPUT/OUTPUT	SIGNAL FUNCTION
Command/Status Present	Output (Active Low)	• Active for Cmd in remote mode • Active for status in master mode • Used with illegal cmd or cmd/status data • See BIU #1 timing
Interrupt Request	Output (Active Low)	• Active level indicates interrupt • Clear interrupt by loading processor control word to run condition
On-Line/Off-Line	I/O (Low Active)	• Pulse from "on line" BIU #2 after entering run condition • Synchronizes "off line" BIU #2 in redundant operation
Select (IW2 Bit 6)	Output (Positive Logic)	• Reflects state of instruction word 2 bit-6 after IW2 DMA is complete
Control Code Control Code Strobe	Input (Positive Logic) Input (Active Low)	• Codes 0000 → 0110 activate interface buffer to accept a 16-bit word from host • Codes 1000 → 1110 activate interface buffer to output a 16-bit word to the host • Code 0111 causes the BIU to interrupt after message is complete • Code 1111 causes the BIU to cease operation and interrupt at the time of the strobe • See BIU module timing • No host DMA action

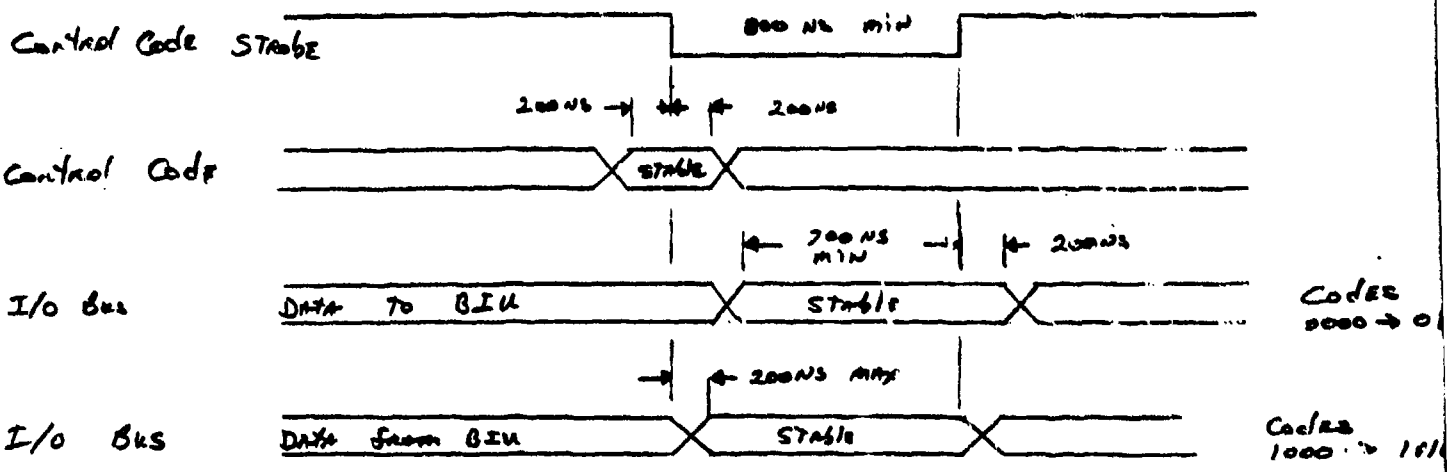


Timing for External Use of Command/Status



DMA Cycle

Figure 1.3.5.3 BIU Module Timing



Control Code Timing

Note : DMA WRITE & DMA READ is gated ON the module with DMA Grant. Internal To the module write & read switch with control codes but do NOT appear AT the module / Host interface because the Request/ Grant SEQUENCE does NOT get inverted.

Note : PLEASE REVIEW and understand BIU # 1 and BIU # 2 Timing before designing with the above data.

Figure 1.3.5.3 (Cont) BIU Module Timing

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AIR FORCE RESEARCH LABORATORY
WRIGHT-PATTERSON AIR FORCE BASE OHIO 45433

26 March 2001

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2. Please change distribution statement on this report *from* Distribution Statement B (US Government agencies only) *to* Distribution Statement A (Approved for public release, distribution unlimited).

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